Contents

Introduction

The manual *Technical equipment of TC600 programmable logic controllers* provides information necessary for proper application, operation and maintenance of basic modules of programmable logic controllers Tecomat TC601 to TC607, extension modules TC621 to TC626 and half extension modules TC631 to TC634. It describes possibilities of the building, differences in technical equipment of individual types, technical parameters of electronic circuits, control and diagnostics and it determines requirements for transportation, storage and installation of the system. Out of data necessary for programming, the manual contains only description of the way of declaration of individual types in an integrated development environment and servicing of inputs and outputs. The very description of the development environment for programming of Tecomat programmable logic controllers is a part of the development environment. The principle of the programmable logic controller function, programming principles and the instruction file of Tecomat programmable logic controllers are described in detail in the *Handbook of the Tecomat PLC programmer, TXV 001 09.02* and *Instruction set of the Tecomat PLC, TXV 001 05.02*. Detailed description of modes of serial communication channels is given in the handbook Serial communication of Tecomat programmable logic controllers, TXV 001 06.02.

With regard to high inheritance of properties of individual types of this series, majority of data is given together for the whole series. Parameters are given individually in the case that parameters of a series type differ.

1. Abbreviations and Terms

PLC	**P**rogrammable **L**ogic **C**ontroller
CPU	PLC **C**entral **P**rocessor **U**nit
CH1, CH2, CH3	PLC Serial **Ch**annels
RTC circuit	**R**eal **T**ime **C**lock, circuit for generation of real time
Tecomat	registered trademark of PLC Teco a. s.
Tecomat TC600	marking of PLC of the TC600 series (TC601-TC607, TC621-TC626, TC631-TC634)
Tecoreg	registered trademark of Teco a. s. regulators
Programmable Logic Controller (PLC)	freely distributable programmable system designed for logic control of work machines, technological processes, etc.
Basic Module (BM)	smallest fully functional set of the PLC
Extension Module (EM, EM/2)	module designed for extension of functional possibilities of the PLC basic module by additional inputs and outputs
RAM Memory	**R**andom **A**ccess **M**emory, memory type for reading and writing
EEPROM Memory	**E**lectrically **E**rasable and **P**rogrammable **R**ead **O**nly **M**emory, memory type for reading
User Program Memory	part of the PLC RAM memory assigned for storage of the user program, data and tables
User Program Source Memory	power independent PLC memory designed for storage of the source (backup) user program, data and tables
User Process	part of the user algorithm assembled by the user from instructions of the problem oriented language of the PLC. Every user process is inclosed in instructions P and E of a common number (0 to 64)

User Program — set of all user processes designed for control of the given application

Multiprogramming — set of rules according to which individual user processes are activated

Program Cycle — set of user processes which are activated cyclically according to rules of multiprogramming

Cycle Turn — phase of the system program between the last process of the past cycle and the first process of the new cycle. In the cycle turn, values of outputs are transmitted from registers Y, new values of inputs are scanned into registers X, time data in timers and system registers are updated, and data received by communication channels and new data for transmission are transferred

Cycle Interruption by User — updating of processes P41, P43 and P44. These processes may be activated in arbitrary position of the user program cycle.

Initialization Processes — processes activated after turning on or restart of the system (P62 after warm reboot, P63 after cold reboot)

User D Data — constants of the user program stored in memory of the user program

User T Tables — most often constants of the user program concentrated in integrated sets (T tables). They are usually used for definition of subsystems (decoders, combination, sequential, time or numeric subsystems).

Configuration Constants, K Data — set of data in the user program memory designed for setting of the system configuration and modification of the system activity. Not available to the user program, are edited from within the development environment. If not edited, the system shows standard behaviour.

Scratchpad, Registers X, Y, S, R — part of the RAM memory available to the user as input images (registers X), output images (registers Y), system (S) and user (R) registers.

Remanent Part of the Scratchpad — part of registers R the contents of which is retained during warm reboot. The extent may be selected by the configurational constant of remanent registers R. Other registers R and registers X and Y are not remanent and are reset in every reboot or turning on. The user has the possibility to store actual output values in remanent registers R.

Warm Reboot — way of activation of the system and user program in which the contents of the scratchpad remanent part are retained. The rest of the scratchpad is reset.

Cold Reboot — way of activation of the system and user program in which all registers of the scratchpad are reset. Cold reboot is performed in the case that an attempt at warm reboot has been non-successful (the system has detected damage of the stored data).

2. Description

2.1 The Specification

PLC's of the TC600 series are freely programmable logic systems designed for control of work machines and technological processes in various and diverse areas of production. They complement the integrated series of modular and compact Tecomat PLC's with a small modular system equipped with the drive for mounting on a U strip.

2.2 Compatibility

Although PLC's of the TC600 series are designed for the smallest applications, use properties of large Tecomat PLC's remain retained. Significant property is uniformness of technical and program means for creation and debugging of the user program and uniformness of the highly efficient instruction set and system services with other Tecomat PLC's allowing for evaluation of experience gained in applications of other Tecomat systems.

2.3 Communication

Two serial communication channels fitted in a standard manner with optional interfaces and possibility of addition of a third communication channel allow for simultaneous local connection of intelligent peripheries equipped with a serial communication channel (readers of the bar code, printers, frequency converters etc.), connection of the operation board and connection to a computer with the development environment or interconnection of individual PLC's in the EPSNET industrial network. Up to 32 Tecomat PLC's, Tecoreg regulators or other devices can participate in the network which meet requirements of the EPSNET network (data terminals, laboratory apparatuses etc.).

2.4 Distributed Control

Using the communication possibilities, it is possible to create extensive systems with distributed control by gradual connecting of autonomous systems to the network and by completion of the program shell without the necessity to intervene in the PLC's technical equipment. Another possibility is additional interconnection of PLC's and collection of data for the central monitoring purposes.

2.5 The Building

The smallest fully functional PLC unit of the TC600 series is formed by the basic module (BM). It is produced in six designs which differ in the number and type of inputs and outputs.

Order numbers for BM PLC of the TC600 series

Type	Order Number [1]	Note			
		Binary inputs	Analog inputs	Transist. outputs	Relay outputs
TC601	TXN 061 51	12	-	8	-
TC602	TXN 061 52	20	-	16	-
TC603	TXN 061 53._ _	12	-	4	4
TC604	TXN 061 54._ _	16	-	-	10
TC605	TXN 061 55._ _	12	4	-	8
TC606	TXN 061 56._ _	16	4	4	10
TC607	TXN 061 57._ _	20	-	20	-

[1] In types TC603 to TC607, the after-number (two digits after the dot) determine the special BM function:
.00 common function of binary inputs (after-number need not be given)
.01 4 interruption binary inputs
.03 measuring by incremental position scanner
.05 counter of type 3 (unidirectional 16 bit counter with pre-selection)
.06 period and phase shift measurement

Optional part of all BM types are interfaces of two serial communications channels (CH1, CH2) fitted in the standard design, additional data memory (DataBox), and a third serial communication channel (CH3) or analog outputs.

Order numbers of optional BM piggybacks

Type	Order number	Note
MR-02	5XK 068 91	Interface RS-232 without galvanic separation from internal control circuits
MR-04	5XK 068 93	Interface RS-485 without galvanic separation from internal control circuits
MR-09	TXK 085 03	Interface RS-485 with galvanic separation from internal control circuits
MR-17	TXK 085 11	Interface RS-422 without galvanic separation from internal control circuits
IM-70	TXK 080 10.00	DataBox, additional data memory 128 kB [1]
IM-70	TXK 080 10.02	DataBox, additional data memory 512 kB [1]
MR-14	TXK 085 08.02	CH3 with interface RS-485 without galvanic separation from internal control circuits [2]
MR-15	TXK 085 09.02	CH3 with RS-232 without galvanic separation from internal control circuits [2]
OT-13	TXK 082 60	4 analog outputs without galvanic separation from internal control circuits [2]
OT-14	TXK 082 61	8 analog outputs without galvanic separation from internal control circuits [2]

[1] DataBox is added in the production plant exclusively
[2] Only 1 piggyback MR-xx or 1 piggyback OT-xx may be fitted

Number of binary and analog inputs and binary outputs of the BM can be extended by connecting one extension module (EM), two half extension modules (EM/2) or by combination of EM, EM/2.

Order numbers of EM and EM/2, PLC of the TC600 series

Type	Order number	Note			
		Binary inputs	Analog inputs	Transist. outputs	Relay outputs
TC621	TXN 061 71	12	-	8	-
TC622	TXN 061 72	20	-	16	-
TC623	TXN 061 73	12	-	4	4
TC624	TXN 061 74	16	-	-	10
TC625	TXN 061 75	12	4	-	8
TC626	TXN 061 76	16	4	4	10
TC631	TXN 061 81	8	-	8	-
TC632	TXN 061 82	8	-	-	8
TC633	TXN 061 83	16	-	-	-
TC634	TXN 061 84	-	8	-	-

2.6 Design

Modules of PLC's of the TC600 series are designed as devices to be built in, designed to be mounted on a U strip, norm ČSN EN 50022 (idt EN 50022:1977). Metal jacket of the modules and mechanical arrangement guarantees higher resistance against interferences.

BM electronic circuits are realized on two printed wiring boards; the central unit and input and output unit.

EM's are fitted with the input and output unit only.

3. Parameters Overview

3.1 Basic Properties

Number of inputs and outputs of PLC TC600 series

	TC601 TC621	TC602 TC622	TC603 TC623	TC604 TC624	TC605 TC625	TC606 TC626	TC607
Binary inputs							
Total number of inputs	12	20	12	16	12	16	20
Arrangement (no. of groups x no. of inputs)	1x8, 1x4	2x8, 1x4	1x8, 1x4	2x8	1x8, 1x4	2x8	2x8, 1x4
Binary transistor outputs							
Total number of outputs	8	16	4	-	-	4	20
Arrangement (no. of groups x no. of outputs)	1x8	2x8	1x4			1x4	2x8, 1x4
Binary relay outputs							
Total number of outputs	-	-	4	10	8	10	-
Arrangement (no. of groups x no. of outputs)			1x4	2x4, 2x1	2x4	2x4, 2x1	
Analog inputs							
Total number of inputs	-	-	-	-	4	4	-
Arrangement (no. of groups x no. of inputs)					1x4	1x4	
	TC601 to TC606						
Analog outputs							
Total number of outputs	4 or 8 - optional						
Arrangement (no. of group x no. of outputs)	1x4 or 1x8						

	TC631	**TC632**	**TC633**	**TC634**
Binary inputs				
Total number of inputs	8	8	16	-
Arrangement (no. of groups x no. of inputs)	2x4	2x4	4x4	
Binary transistor outputs				
Total number of outputs	8	-	-	-
Arrangement (no. of groups x no. of outputs)	1x8			
Binary relay outputs				
Total number of outputs	-	8	-	-
Arrangement (no. of groups x no. of outputs)		2x4		
Analog inputs				
Total number of inputs	-	-	-	8

3.2 Operational Conditions

Class of environment effect	normal according to ČSN 33 2000-3 (mod IEC 364-3:1993)
Range of operational temperatures	0 °C to +55 °C
Average temperature during 24 hours	max. +50 °C
Allowed transportation temperature	-25 °C to +70 °C
Relative air humidity	50 % to 95 % without condensation
Degree of pollution	1 according to ČSN EN 61131-2 (idt EN 61131-2:1992, IEC 1131-2:1992)
Overvoltage category of installation	II according to ČSN 33 0420 (eqv IEC 664:1980, IEC 664A:1981)
Immunity against disturbances	levels according to ČSN EN 61131-2 (idt EN 61131-2:1992, IEC 1131-2:1992) (tab. 16)
Emitted disturbance	levels for group 1, class A according to ČSN EN 55011 (mod CISPR 11:1997)
Vibrations	Fc 10 Hz to 150 Hz, 0.15 mm, 10 cycles according to ČSN EN 60068-2-6 (idt EN 60068-2-6:1995, IEC 68-2-6:1995+Corr.1995)
Operating position	vertical
Type of operation	permanent

3.3 Basic Parameters

	BM	EM	EM/2
Type of appliance	to be built-in		
Class of el. object	I according to ČSN 33 0600 (mod IEC 536-1:1976, IEC 536-2:1992)		
Coverage	IP-10B		
Supply voltage (SELV)	24 V~ ±20 %, 50-60 Hz ±5 % or 24 V- ±20 %		
Power input	max. 20 VA or 13 W [1)]		
Mass	about 0.8 kg	about 0.4 kg	about 0.2 kg
Size (h x w x d) [2)]	141x182x69	141x157x44	141x89x44

[1)] Power input of BM extended by one EM and one EM/2
[2)] See figs. 9.1, 9.2, 9.3

4. Central Unit

4.1 Basic Parts and Parameters

Central unit ensures the majority of PLC control functions. Due to its properties, it is ranked among Tecomat CPU D series. It contains especially the supply voltage converter, microcontroller, memories RAM and EEPROM, RTC circuit, lithium battery to supply voltage to the RAM memory and RTC circuit in the case that the PLC power supply is turned off, two serial communication channels and optional additional data memory and analog output circuits or a third serial communication channel.

CPU Basic parameters

Central unit series	D
Real time circuit (RTC)	fitted in standard design
User program source memory	fitted in standard design
Memory type	EEPROM (FLASH)
Memory size	32 kB
User program and data memory	fitted in standard design
Memory type	RAM
Memory size	32 kB
Additional data memory, DataBox	optional
Memory type	RAM
Memory size	128 kB or 512 kB
Backup of the RAM memory and RTC	min. 20 000 h
Cycle period per 1k of logic instructions	13 ms
Total number of user registers	8 192
Number of remanent registers	optional 0 to 512
Total number of timers and counters	4 096
Range of timers	65 536 x 10 ms to 10 s, possibility of cascading
Range of counters	65 536, possibility of cascading
Instruction set	extended
Instruction length	1 to 6 bytes
Number of serial communication channels	2 + 1, optional
Transmission speed of CH1, CH2, CH3	0.3 to 230.4 kBd [1)]
Number of analog outputs	optionally 0, 4 or 8

[1)] Maximum transmission speed is limited by the maximum allowed transmission speed of the set communication channel mode.

4.2 User Accessible Memories

User program memory

Memory of the user program is formed by a part of the RAM memory of CPU assigned for the user program, data and tables. When PLC is turned off, the memory is supplied by the built-in lithium battery.

User program source memory

Source memory of the user program is formed by a part of the EEPROM memory of CPU assigned for saving of a copy of the user program. The memory power-independent, that is, contents of the memory remain retained even after the power supply of the PLC is turned off or when the battery is discharged. Use of the source memory is controlled by the user by setting a parameter in the PLC SET mode (see Article 4.5).

When the source memory is allowed, after exiting the SET mode, turning on of the PLC power supply or restart, contents of the user program source memory is moved to the user program memory with which CPU works. The function is used especially for backup of the user program. The memory is programmed from within the development environment directly in the PLC.

Memory of CPU parameters

Memory of CPU parameters is power-independent memory designed for storage of parameters that can be set in the PLC SET mode. Contents of the memory remain retained even when the PLC power supply is turned off or if the battery is discharged.

Scratchpad memory

The scratchpad memory is a part of the CPU RAM memory accessible to the user in the form of input images (registers X), outputs images (registers Y), system (S) and user registers (R). Preserving of the scratchpad contents after turning off of the PLC power supply and restarts is program-controlled. The behaviour is described in detail in Chapter 10.

The DataBox

The DataBox is an optional complement of the CPU, fitted by the producer on the basis of an order. It extends the user accessible RAM memory by 128kB or the data memory by 512kB. When the PLC is turned off, the memory is supplied from a built-in lithium battery. It is designed for working with greater amounts of data, for example for archiving of data on the controlled process for a longer time period etc. The data can be written to the memory or read, respectively, either by using the PLC user program or through the serial line.

Support of working with the DataBox

For support of the DataBox program attendance, there are three user instructions available. The READDBX instruction is intended for reading of data from DataBox into R registers, the WRITEDBX instruction is intended for writing of data from R registers to the DataBox, and the SIZEDBX instruction serves for identification of the DataBox size. Detailed description of function of instructions, their definitions, structures of the parameters zone for instructions READDBX and WRITEDBX and way of calling of instructions in the user program are given on the distribution diskette xPRO which forms a part of the PLC delivery.

For serial communication with the DataBox, either CH1 can be used which always operates in the PC mode or channels CH2, CH3 set in the PC mode. To support serial communication with the DataBox, the COMPLC.EXE program is available which allows for reading data from DataBox into a file or write data from a file to DataBox, respectively, and test size of memory accessible in the form of the DataBox. Working with the DataBox is possible starting from the COMPLC.EXE program version 1.6. The program, which is found on the xPRO distribution diskette, must be run under the MS DOS operating system.

Backup of the RAM memory and RTC circuit power supply

When the PLC power is turned off, the RAM memory and RTC circuit are supplied from a built-in lithium battery. Parameters of the used battery allow for backup with the power supply turned off for the minimum time of 20000 hours. In common operating conditions (operating temperature of 20 °C, unidirectional operation at least) and typical power take-off of the backing circuits, the backup time is limited by battery life (5 years at the minimum).

Detection of state of the backup battery

Voltage of the backup battery is evaluated by the diagnostic system. In the case the voltage drops under 2.5 V, bit .0 of the S35 system register is set to the state log. 1. PLC continues with its activity until the voltage drops under the minimum supply voltage of the RTC circuit. Evaluation of the RTC circuit failure leads to bringing the PLC in the HALT mode and announcing the error message 80 0C 00 00.

4.3 Analog Outputs

Analog outputs are used for control of voltage-control action elements of the controlled object. They are arranged in a group with a common terminal of the analog ground. Analog outputs are galvanically connected with the CPU control circuits. Physically, the analog outputs are realised on small plug-in units, the so called piggybacks, fitted on the CPU if ordered. Number of outputs depends on the type of the chosen piggyback (see Article 2.5).

Parameters of analog outputs

	OT-13	OT-14
Number of output channels	4	8
Arrangement of outputs	1x4	1x8
Common group conductor	minus	
Galvanic separation from internal control circuits	no	
Type of output	voltage	
Voltage range/resolution (1 LSB [1)])	÷0 to 9.96 V/ 39 mV	
Error of output voltage	typ. ± 1 LSB max. ± 4 LSB	
Binary output representation	8 bits	
Output current	max. 10 mA	
Setting time of the output	max. 30 μs	
Output load resistance	>1 kΩ	
Resistance against short-circuit	min. 5 s	

[1)] LSB (Least Significant Bit) - lowest bit of the binary value

$$1\ \text{LSB} = \frac{10\text{V}}{2^8}$$

4.4 Serial Communication Channels

Standard design of all PLC's of the TC600 series is equipped with two communication channels. Third communication channel is added per order (see Article 2.5).

4.4.1 Serial Communication Channel 1 (CH1)

To program the PLC, communication channel CH1 is used

CH1 is designed for connection of the PLC to a superior system. The superior system most often represents a computer of the PC class performing the function of a programming device, visualisation station or control device of the PLC network. It contains a complete set of the EPSNET network services. Detailed description of the services is given in the handbook *Serial Communication of Tecomat Programmable Logic Controllers, TXV 001 06.02.*

Interface RS-232 of CH1 is activated after connection of the interconnecting cable TXK 646 51.06

CH1 is equipped with fixed fitted interface RS-232 without galvanic separation from internal circuits. Besides this, in all types of BM, CH1 can be complemented with a piggyback with interface RS-485 or RS-422. Optional interface is implicitly assigned to CH1. Interface RS-232 is assigned to CH1 automatically by connecting the cable TXK 646 51.06. Together with connecting interface RS-232, the optional interface (if fitted) is disconnected from CH1. For selection of the interface type, especially function of the superior device is decisive, type of interface of its serial communication channel, connection distance, transmission speed and level of disturbances.

4.4.1.1 Interface RS-232

Interface RS-232 is used for two-point connection

Interface RS-232 ensures conversion of output signals of TTL level to level defined by the specification V.28 (EIA RS-232), and of input signals according to V.28 to the TTL level. It allows for connection of two end devices in the duplex mode. It is suitable for connection realised in short distance in an environment with low level of electromagnetic disturbances.

For the communication, PLC's of the TC600 series use only binding circuits of signals TxD (Transmit Data), RxD (Receive Data), CTS (Clear To Send), and RTS (Request To Send) of the standard RS-232 interface.

Parameters of the RS-232 interface

Transmission speed	max. 230.4 kBd [1)]
Cable length	max. 15 m [2)]
Voltage of outputs TxD, RTS for level 1	typ. -8 V against GND (R_l=5 kΩ)
Voltage of outputs TxD, RTS for level 0	typ. +8 V against GND (R_l=5 kΩ)
Voltage of inputs RxD, CTS for level 1	min. -3 V against GND max. -25 V against GND
Voltage of inputs RxD, CTS for level 0	min. +3 V against GND max. +25 V against GND
Impedance of inputs RxD, CTS	5 kΩ

1) The maximum transmission speed is limited by the maximum allowed transmission speed of the set mode of the communication channel.

2) The maximum cable length may only be used provided that the maximum transmission speed is reduced.

4.4.1.2 Interface RS-485

Interface RS-485 is used for multi-point connection

Interface RS-485 ensures conversion of output signals of the TTL level to level defined by the specification V.11 (X.27, EIA RS-485), and input signals according to V.11 to the TTL level. Parameters of symmetric binding circuits of the RS-485 interface allow for multi-point connection of end devices in the half-duplex mode. It is suitable for connection realised in medium distance in an environment with higher level of electromagnetic disturbances.

For the communication, PLC's of the TC600 series use binding circuits of signals TxD (Transmit Data), RxD (Receive Data). Signal RTS (Request To Send) is used internally for control of the transmitter activation.

Parameters of the RS-485 interface

Transmission speed	max. 230.4 kBd [1)]
Cable length	max. 1200 m [2)]
Sensitivity of differential inputs RxD+, RxD-	±200 mV
Input resistance of differential inputs RxD+, RxD-	min. 12 kΩ
Voltage of differential inputs	min. 0.2 V
RxD+, RxD- for level 1	max. 12 V
Voltage of differential inputs	min. -0.2 V
RxD+, RxD- for level 0	max. -7 V
Voltage of differential outputs	min. 1.5 V (R_l=75Ω)
TxD+, TxD- for level 1	max. 5 V (Io=0)
Voltage of differential outputs	min. -1.5 V (R_l=75Ω)
TxD+, TxD- for level 0	max. -5 V (Io=0)
Difference of the output voltage value for levels 0 and 1	max. ±0.2 V
Output current	max. ±250 mA

1) The maximum transmission speed is limited by the maximum allowed transmission speed of the set mode of the communication channel.

2) The maximum cable length may only be used provided that the maximum transmission speed is reduced.

4.4.1.3 Interface RS-422

Interface RS-422 is used for two-point connection

Interface RS-422 of PLC's of the TC600 series ensures conversion of output signals of the TTL level to level defined by the specification V.11 (X.27, EIA RS-422), and input signals according to V.11 to the TTL level. Parameters of symmetric binding circuits of the RS-422 interface allow for two-point connection of end devices in the duplex mode. It is suitable for connection realised in medium distance in an environment with higher level of electromagnetic disturbances.

For the communication, PLC's of the TC600 series use only binding circuits of signals TxD (Transmit Data) and RxD (Receive Data) of the RS-422 interface.

Parameters of the RS-422 interface

Transmission speed	max. 230.4 kBd [1)]
Cable length	max. 1200 m [2)]
Sensitivity of the differential input RxD+, RxD-	±200 mV
Input resistance of the differential input RxD+, RxD-	min. 12 kΩ
Voltage of the differential input	min. 0.2 V
RxD+, RxD- for level 1	max. 12 V
Voltage of the differential input	min. -0.2 V
RxD+, RxD- for level 0	max. -7 V
Voltage of the differential output	max. 5 V (Io=0)
TxD+, TxD- for level 1	2.3 V (R_l=100 Ω)
Voltage of the differential output	max. -5 V (Io=0)
TxD+, TxD- for level 0	-2.3 V (R_l=100 Ω)
Difference of the output voltage value for levels 0 and 1	max. ±0.2 V
Output current	max. ±60 mA

1) The maximum transmission speed is limited by the maximum allowed transmission speed of the set mode of the communication channel.

2) The maximum cable length may only be used provided that the maximum transmission speed is reduced.

4.4.2 Serial Communication Channel 2 (CH2)

CH2 is designed for general use

CH2 serves especially for connection of intelligent peripheries with a serial input or output of data to the PLC, and for mutual interconnection of PLC's. It can operate in several modes:

Mode **PC** - connection of a superior system, usually a PC
Mode **PLC** - interconnection of PLC's or regulators for mutual transfer of data
Mode **MAS** - data collection from subordinate PLC's or regulators in the EPSNET network
Mode **uni** - general user channel for universal use

Setting of the required mode is given in Article 4.5, detailed description of the modes is given in the handbook *Serial Communication of Tecomat Programmable Logic Controllers, TXV 001 06.02.*

CH2 interface is optional (see Article 2.5). Parameters of the interface are given under item 4.4.1.

4.4.3 Serial Communication Channel 3 (CH3)

CH3 is designed for general use

CH3 is an optional part of the PLC. It can be complemented only in types without analog outputs. It serves especially for connection of intelligent peripheries with a serial input or output of data or connection of an external control board, mutual interconnection of PLC's or connection of a PLC to a superior system. It can operate in several modes:

Mode **PC** - connection of a superior system, usually a PC
Mode **PLC** - interconnection of PLC's or regulators for mutual data transfer
Mode **MAS** - data collection from subordinate PLC's or regulators in the EPSNET network
Mode **uni** - general user channel for universal use

Setting of the required mode is given in Article 4.5, detailed description of the modes is given in the handbook *Serial Communication of Tecomat Programmable Logic Controllers TXV 001 06.02.*

CH3 interface is dependent on the type of the communication piggyback (see Article 2.5). Interface parameters are given under item 4.4.1.

4.5 Setting of CPU Parameters

Mode SET

CPU parameters are set in the setting mode (mode SET). To set and display parameters, the PLC front board is equipped with buttons SET and MODE and a one-place seven-segment LED display.

Displaying of parameters

In the SET mode, all data are displayed in the rotational way, that is, number 123 is displayed in such a way that digits 1, 2, 3 are lighted gradually on the display, then there is a delay, and the whole sequence is repeated. Every character is displayed for about 0.5 s and is separated from the following character by a delay which ensures recognition of two identical characters displayed one after another (for example, displaying of the number 111).

Entrance in the SET mode

Switching to the SET mode can be performed by pressing buttons SET and MODE simultaneously while the PLC power supply is on. Buttons SET and MODE are held pressed until the triple dash ≡ appears on the display. In general it holds that by the SET button we change setting of the parameter, and by the MODE button we move through individual parameters. Pressing of the button is indicated by lighting of the decimal point on the display.

Termination of the SET mode

The SET mode may be terminated any time by simultaneously pressing the buttons SET and MODE. We again hold the buttons SET and MODE pressed until the triple dash ≡ appears on the display. State of parameters is saved upon termination of the mode in the power-independent memory of parameters, and the PLC switches to the HALT mode or some of error messages may possibly be signalled.

Adjustable parameters

Tab. 4.1 Adjustable CPU parameters
(ordered from the left to the right and in the rows)

Object to be set	**Adjustable parameters**				
channel CH1	-	address	speed	delay of reply	CTS detection
channels CH2 and CH3 [1)]	off	-	-	-	-
	mode **PC**	address	speed	delay of reply	CTS detection
	reg. **PLC**	address	speed	-	-
	mode **MAS**	-	speed	transport delay	CTS detection[2)]
	reg. **uni**	-	-	-	-
Program source memory	off				
	on				

[1)] Only BM's fitted with the communication piggyback contain channel CH3.

[2)] CTS detection in the MAS mode cannot be set for CH3.

4.5.1 Setting of Parameters of Serial Communication Channels CH1, CH2, CH3

Setting of the serial channel mode

Channel CH1 has fixed-set mode PC which cannot be changed. In this channel, the parameter serial channel mode is not set.

In setting the parameter serial channel mode for channels CH2, CH3, a message of the following type is shown on the display

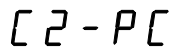
with the following meaning:

C - setting of the serial channel mode
2 - number of the channel being set
off - the mode being set

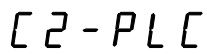
Serial channels may operate in the following modes:

off - channel is off (no other channel parameter is set)

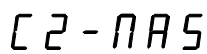
PC - connection of a superior system (a PC or an active operation board)



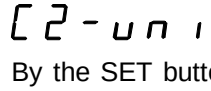
PLC - interconnection with other PLC's or regulators in the EPSNET multimaster network with fast data exchange



MAS - data collection from subordinate PLC's or regulators in the EPSNET network



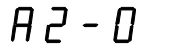
uni - general user channel for universal use



By the SET button we move through individual modes. By pressing the MODE button we save the set mode and move to setting of another parameter

Setting of the serial channel address

When setting the parameter **serial channel address**, a message of the following type is shown on the display



with the following meaning:

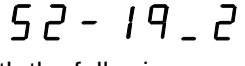
A - setting of the serial channel address
2 - number of the channel being set
0 - the set address

Address may take a value from 0 to 99. By shortly pressing the SET button, we increase its value by 1, by pressing and holding the SET button (for about 1s) we increase its value by 10. By pressing the MODE button, we save the set value and move to setting of another parameter.

Address is set only for modes **PC** and **PLC**. In the uni mode, setting of the address is a part of the initialisation table in the user program.

Setting of the serial channel communication speed

When setting the parameter serial channel communication speed, a message of the following type is shown on the display



with the following meaning:

S - setting of the serial channel communication speed
2 - number of the channel being set
19_2 - set speed in kb/s (the underscore is a substitute for the decimal point)

The speed may take values defined in advance according to table 4.2. Speed not available in the given mode of the given channel, is not offered when browsing by the SET button. By pressing the MODE button, we save the set value and move to setting of another parameter.

The speed is set only for modes **PC**, **PLC** and **MAS**. In the uni mode, speed setting is a part of the initialisation table in the user program.

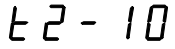
Tab. 4.2 List of available transmission speeds of CH1, CH2 and CH3 in various modes

Speed	Channel mode
0.3 kb/s	PC,MAS
0.6 kb/s	PC,MAS
1.2 kb/s	PC,MAS
2.4 kb/s	PC,MAS
4.8 kb/s	PC,MAS
9.6 kb/s	PC,PLC,MAS
14.4 kb/s	PC,PLC,MAS
19.2 kb/s	PC,PLC,MAS

Speed	Channel mode
28.8 kb/s	PC,PLC,MAS
38.4 kb/s	PC,PLC,MAS
57.6 kb/s	PC,PLC,MAS
76.8 kb/s	PLC
115.2 kb/s	PLC
172.8 kb/s	PLC
230.4 kb/s	PLC

Setting of the reply delay and transport delay

When setting the parameter **reply delay** (in the **PC** mode) or **transport delay** (in the **MAS** mode), a message of the following type is shown on the display



with the following meaning:
t - setting of the reply delay
2 - number of the channel being set
10 - set delay/transport delay in ms

By shortly pressing the SET button, we increase the value of the delay/transport delay by 1, by pressing and holding the SET button (for about 1s) we increase its value by 10. By pressing the MODE button we save the set value and move to setting of another parameter.

Reply delay

Optional reply delay serves for solution of situations when the superior system sending the message, cannot switch in time from transmission mode to receiving mode, and thus it cannot receive the PLC's reply. By extending the reply delay the superior system gains time for preparation necessary to start receiving of a reply.

The delay time is set in ms and may take values from 0 to 99 ms. Value 0 means that the minimum reply delay shall correspond with the time necessary to transmit 1 byte, thus it depends on the set speed. Values 1 to 99 give the delay in milliseconds and are not dependent on the communication speed.

The reply delay is set only for mode **PC**.

Transport delay

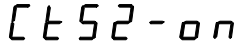
Optional transport delay serves for solution of situations when the PLC in the role of the superior system is waiting for reply from a subordinate PLC for longer than 0.5 s for the reason of delay on the transmission line, caused by modems etc.

Transport delay is set in multiples of 100 ms and may take values from 0 to 6 s. Value 0 means that the superior PLC waits for the reply for the maximum of 0.5 s (time of cycle of the subordinate PLC may not exceed this value). Values 1 to 60 give the transport delay of 0.1 to 6 s which is added to the value 0.5 s. Values 61 to 99 set the maximum transport delay of 6 s.

The transport delay is set only for mode **MAS**.

Setting of the CTS signal detection

When setting the parameter **CTS signal detection**, a message of the following type is shown on the display



with the following meaning:
CTS - setting of the CTS signal detection
2 - number of the channel being set
on - detection on

Detection of the CTS signal may be either off or on. By pressing the SET button we change the setting, by pressing the MODE button we save the set value and move to setting of another parameter.

When detection of the CTS signal is on, before transmission of the reply the PLC tests state of the CTS signal after setting the RTS signal. The reply is transmitted only if the CTS signal has the same value as the RTS signal. This mode is suitable for communication via modems. The set reply delay holds in this mode too, it is thus ensured that PLC shall not reply before the delay elapses even if the CTS signal is already set.

When CTS signal detection is off, PLC controls the RTS signal but does not take into consideration state of the CTS signal.

Detection of the CTS signal can be set for the **PC** mode of all channels and for the **MAS** mode for channel CH2. For channels CH2 and CH3 in the uni mode, detection of the CTS signal can be set using the initialisation table in the user program.

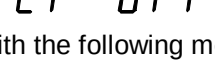
Default setting of parameters

Parameters of CH1 are implicitly set by the producer to the following values: mode - PC, address - 0, speed - 19.2 kb/s, delay - 0, CTS detection - off

CH2 and CH3 are implicitly off.

4.5.2 Management of the user program source memory

When setting parameters of the source memory, a message of the following type is shown on the display



with the following meaning:
EP - setting of the user program source memory
off - memory off (default value)

The source memory may be either off or on. By pressing the SET button we change the setting, by pressing the MODE button we save the set value and move to setting of another parameter.

When the parameter is set to the off value, after the PLC switches to the RUN mode, program stored in the user program memory is run. When the parameter is set to the on value, after the setting mode is ended and in every subsequent turning on of the PLC power supply, program from the source memory is first moved to the user program memory, and this program is then run in the RUN mode. The function serves especially for backing of power-dependant memory of the user program.

5. Input and Output Unit

5.1 Basic Functions

The majority of input and output circuits of the PLC is realized on the input and output unit. Individual types of the series differ in the type of the used input and output unit or in modification of the unit fitting with circuits of binary and analog inputs and binary transistor and relay outputs.

5.1.1 Binary Inputs

Binary inputs serve for connection of two-state signals of the controlled object to the PLC. To increase functional reliability, every input is galvanically separated by an optical element from internal circuits and is equipped with a filter. If the input is excited (closed), this is signalled by lighting of the LED diode. Inputs are organized in groups with one common connector. A group of signals may be connected in one or the other polarity.

Inputs DI1 to DI3 of modules TC603 to TC607 can be used for basic function identical with other inputs or for realization of the PLC special functions.

Parameters of binary inputs

	TC601 TC621	TC602 TC622	TC603 TC623	TC604 TC624	TC605 TC625	TC606 TC626	TC607
Total number of inputs	12	20	12	16	12	16	20
Arrangement (no. of groups x no. of inputs)	1x8, 1x4	2x8, 1x4	1x8, 1x4	2x8	1x8, 1x4	2x8	2x8 1x4
	TC631	TC632	TC633	TC634			
Total number of inputs	8	8	16	-			
Arrangement (no. of groups x no. of inputs)	2x4	2x4	4x4				
Group common conductor	plus or minus						
Galvanic separation from other electric circuits	yes						
Nominal voltage	24 V-, 24 V~						
Voltage for log. 0	max. 12 V-, 11 V~ (max. 14 V-, 13.5 V~) [1)]						
Voltage for log. 1	min. 16 V-, 15 V~ (min. 18.5 V-, 17.5 V~) [1)] max. 30 V-, 30 V~						
Current for log. 1	typ. 10 mA						
Delay from log. 0 to log.1	typ. 4 ms						
Delay from log. 1 to log.0	typ. 4 ms						
Pulse overload capacity of the input	max. 250 V (pulse width 100 μs, period 1 s)						

[1)] Value valid for inputs DI0 to DI3 of modules TC603 to TC607 and TC623 to TC626

5.1.2 Binary Transistor Outputs

Binary transistor outputs serve for control of two-state action and signalling elements, which require high count and el. closing speed. To increase functional reliability, every output is galvanically separated by an optical element from internal circuits and is protected against short circuit, overvoltage and reversing of polarity.

When connecting an external power supply of outputs, closing of individual outputs is signalled by lighting of the LED diode. By lighting, the common LED diode marked as BLK, signals blocking of outputs in the still (open) state.

Outputs are organized in groups with one common connector.

Parameters of transistor outputs

	TC601 TC621	TC602 TC622	TC603 TC623	TC604 TC624	TC605 TC625	TC606 TC626	TC607
Total number of outputs	8	16	4	-	-	4	20
Arrangement (no. of groups x no. of outputs)	1x8	2x8	1x4			1x4	2x8 1x4
	TC631	TC632	TC633	TC634			
Total number of outputs	8	-	-	-			
Arrangement (no. of groups x no. of outputs)	1x8						
Group common conductor	plus						
Galvanic separation from other electric circuits	yes						
Operational voltage of outputs	9.6 V- to 28.8 V-						
Current of outputs	max. 1 A						
Current of the common conductor	max. 6 A		max. 4 A				6 A 4 A
Residual current in el. opening	max. 300 μA						
El. closing time	max. 400 μs						
El. opening time	max. 400 μs						
Protection against short circuit	yes						
Limitation of the initial peak current	typ. 7.5 A						
Disconnecting time of the initial peak current	typ. 4 ms						
Limitation of short circuit current	typ. 4 A						
Protection against overload	yes						
Current limitation	typ. 4 A						
Protection against reversing of polarity	yes [1)]						
Servicing of inductive load	external						

[1)] The circuit is brought in non-active state, loads are closed, current will flow through the circuit protective diode.

5.1.3 Binary Relay Outputs

Binary relay outputs serve for control of two-state action and signalling elements of the controlled object, supplied by alternating voltage or voltage higher than the allowed range of closed voltage of transistor outputs. Outputs are realized by the closing voltage-free contact relay led out independently or in a group with one common connector.

Closing of every output is signalled by lighting of the LED diode. The common LED diode marked as BLK, signals by lighting blocking of outputs in the still (open) state.

Parameters of relay outputs

	TC601 TC621	TC602 TC622	TC603 TC623	TC604 TC624	TC605 TC625	TC606 TC626
Total number of outputs	-	-	4	10	8	10
Arrangement (no. of groups x no. of outputs)			1x4	2x4, 2x1	2x4	2x4, 2x1
	TC631	TC632	TC633	TC634		
	-	8	-	-		
		2x4				
Galvanic separation from other electric circuits	yes					
Contact parameters						
Closed voltage	max. 250 V ≅					
Closed current	max. 1 A					
Closed alternating output	max. 250 VA					
Closed direct-current output	max. 24 W for voltage 24 V max. 43 W for voltage 48 V max. 57 W for voltage 250 V					
Current through the group common conductor	max. 4 A					
Closing and opening time	typ. 5 ms					
Oscillation time	typ. 1 ms					
Mechanical life	min. 20 x 10^6 closings					
Servicing of inductive load	external					
Protection of the contact against overload	external					
Dielectric resistance of the open contact	1 kV~					
Dielectric resistance between relay contacts and non-live PLC parts	2.2 kV~					
Dielectric resistance between relay contacts and SELV circuits	3.75 kV~					
Dielectric resistance between contact groups[1)]	3.75 kV~					

[1)] Including contacts led out independently

5.1.4 Analog Inputs of TC605, TC606, TC625, TC626 Modules

Analog inputs serve for connection of up to four analog signals of the controlled object to the PLC. They are intended especially for processing of analog signals with normalized current or voltage level. Input circuits are galvanically connected with internal PLC control circuits.

Inputs are arranged in a group with one common connector of the analog ground. Every input can be set individually by a jumper for the voltage or current signal source. The measurement range is set by a program. Type of input and the measurement range can be selected for every input independently of other inputs.

Format of input data

Value of the input variable is passed in the FS format (Full Scale). Value 0 of the input data corresponds with the lower limit of the measurement range, the maximum value of the input data 4095 corresponds with the upper limit of the measurement range. Exceeding of the converter range is not signalled. Conversion to technical units is performed on the user program level. The FS format provides the highest possible resolution.

Parameters of analog inputs TC605, TC606, TC625, TC626

	TC601 to TC604 TC621 to TC624	TC605, TC606 TC625, TC626
Number of input channels	-	4
Arrangement (no. of groups x no. of inputs)		1x4
Group common conductor	minus	
Galvanic separation from internal electric circuits	no	
Input binary representation	12 bits unsigned	
Conversion time of 4 channels	4 ms	
Input type	current or voltage	
Voltage inputs		
Measurement range/ resolution (1 LSB)	0 V to +10 V/ ≐2.44 mV [1] 0 V to +2 V/ ≐0.49 mV [2]	
Input resistance	>10 MΩ	
Recommended internal resistance of the signal source	<10 kΩ	
Current inputs		
Measurement range/ resolution (1 LSB)	0 mA to +20 mA/ ≐4.9 μA	
Input resistance	100 Ω	
Input current	max. 50 mA	
Input voltage	max. 5 V	

LSB (Least Significant Bit) - lowest bit of the binary value

[1] $1\ LSB = \frac{10V}{4095}$

[2] $1\ LSB = \frac{2V}{4095}$

5.1.5 Analog Inputs of the TC634 Module

Analog inputs serve for connection of up to eight analog signals of the controlled object to the PLC. They are intended especially for measurement of temperatures using passive resistance temperature scanners, and for processing of analog signals with normalized current or voltage level. Input circuits are galvanically connected with the PLC internal control circuits.

Inputs are fixed-configured as differential ones. Every input can be set individually using a jumper for direct-current voltage or current signal source. Measurement range and format of the input variable value are set in a program. Input type, measurement range and format of the value of input data can be selected for every input independently of other inputs.

Switching of the current source allows for connection of two detector strings with impedance up to 8 kΩ

To supply power to passive resistance detectors, an internal power supply providing specific current 1 mA is available, which is switched in measurements automatically to one of the two output clips.

The module ensures filtering off of the disturbance component of input signals, protection of input circuits, conversion of the analog voltage or current input level to the binary value, and conversion of the value into the chosen format.

Parameters of analog inputs of TC634

Number of input channels	8
Arrangement of inputs	8 differential
Method of A/D conversion	sigma-delta modulation
Input filtration	digital filter 50 Hz
Calibration	automatic at the PLC initialization and at every change of the measurement range
Conversion time of one channel	60 ms
Reconfiguration time of one channel [1)]	180 ms
Total measurement time[2)]	variable according to configuration
Input response time[3)]	60 ms
Binary representation of the input	16 bits
Galvanic separation from internal electric circuits	no
Galvanic separation from non-live PLC parts	yes
Input type (can be selected by a jumper)	current voltage voltage - passive resistance scanners of temperature

1) Reconfiguration time of one channel is time necessary to change and calibrate the measurement range and conversion of one channel. It is applied at transferring among different input types.

2) Total measurement time is the sum of times necessary for conversion or reconfiguration of all declared input channels

3) Response time of the input is time which the input signal needs to reach 100% of its final value. If the signal change is faster than the response time of the input, the signal is reduced by the input filter.

Parameters of inputs for TC634 resistance temperature scanners

Scanner type (can be selected by a program)	Pt100 W_{100} = 1.385 Pt100 W_{100} = 1.391 Ni1000 W_{100} = 1.617 Ni1000 W_{100} = 1.500 general 0 to 630 Ω general 0 to 2520 Ω
Measurement range	see table 5.1a
Resolution	see table 5.2a
Format of input data	see table 5.1a
Total measurement error	see table 5.3a
Temperature drift	see table 5.3a
Input resistance	>10 MΩ
Resistance of the signal source	max. 8 kΩ
Input voltage[1)]	max. ± 12 V
Current of the power supply for supplying of scanners	1 mA
Load resistance of the current supply[2)]	max. 8 kΩ

1) Greatest voltage difference measured among all input clips of the module may not exceed this value.

2) The given load may be connected to both output clips of the current supply (IoutA, IoutB).

Parameters of TC634 current inputs

Measurement range (can be selected by a program)	0 mA to +20 mA +4 mA to +20 mA
Resolution	see table 5.2b
Format of input data	see table 5.1b
Total measurement error	see table 5.3b
Temperature drift	see table 5.3b
Input resistance	25.2 Ω
Input current	max. 50 mA
Input voltage	max. 5 V

Parameters of TC634 voltage inputs

Measurement range (can be selected by a program)	0 V to +10 V 0 V to +2 V
Resolution	see table 5.2b
Format of input data	see table 5.1b
Total measurement range	see table 5.3b
Temperature drift	see table 5.3b
Input resistance	>10 MΩ
Resistance of the signal source	max. 10 kΩ
Input voltage[1)]	max. ± 12 V

1) Greatest difference of voltage measured among all input clips of the module may not exceed this value.

Formats of input data

Value of the input variable is passed in one of three formats. Format of input data is selected in a program.

Format FS

In the FS format (Full Scale), value 0 of input data corresponds with the lower limit of the measurement range, the maximum value of input data 65535 corresponds with the upper limit of the measurement range. Exceeding of the range of the converter is not signalled. Conversion to technical units is performed on the user program level. The FS format provides the highest possible resolution.

Technical units

In the Technical units format, converted value of the input variable is passed in °C, Ω, μA or mV. Exceeding of the range is signalled by value

$7FFF, underflow of the range is signalled by value $-7FFF ($8001). Detailed data on signalling of overflow and underflow of the range for individual types of inputs - see notes to table 5.1.

Format PID

In the PID format, value of the input variable is passed, converted to the format compatible with PID instructions of Tecomat programmable logic controllers. The value can be interpreted as percentage expression of the full measurement range. Exceeding of the range is signalled by the value $7FFF. Detailed data on signalling exceeding of the range for individual input types - see notes to table 5.1.

Format of input data of resistance temperature scanners

Tab. 5.1a. Format of input data of TC634 resistance temperature scanners

Scanner type/ measurement range	Data format			
	FS	Technical units		PID [3]
		tenths of °C[1)2)]	tenths of Ω[3)]	
Pt100, W100 = 1.385 -200 to +850 °C	0 to 65535	-2000 to +8500		
Pt100, W100 = 1.391 -200 to +850 °C	0 to 65535	-2000 to +8500		
Ni1000, W100 = 1.617 -60 to +200 °C	0 to 65535	-600 to +2000		
Ni1000, W100 = 1.500 -60 to +200 °C	0 to 65535	-600 to +2000		
0 to 630 Ω	0 to 65535		0 to 6300	0 to 10000
0 to 2520 Ω	0 to 65535		0 to 25200	0 to 10000

1) At conversion to the format of **°C tenths**, correction of non-linearity of scanners is realized as well according to ČSN IEC 751 (idt EN 60751:1995).
2) For the marked format, value $7FFF signals interruption of the scanner, value $-7FFF ($8001) signals short circuit of the scanner.
3) For the marked format, exceeding of the upper limit of the range is signalled by value $7FFF.

Tab. 5.1b. Format of input data of TC634 current and voltage inputs

Measurement range	Data format				
	FS	Technical units			PID
		µA	mV	tenths of mV	
0 to +20 mA	0 to 65535	0 to 20000 [1)]			0 to 10000 [1)]
+4 to +20 mA	0 to 65535	4000 to 20000 [2)]			0 to 10000 [2)]
0 to +10 V	0 to 65535		0 to 10000 [3)]		0 to 10000 [3)]
0 to +2 V	0 to 65535			0 to 20000 [4)]	0 to 10000 [4)]

1) For the marked format, exceeding of the range at current higher than 22 mA is signalled.
2) For the marked format, exceeding of the range at current higher than 22 mA is signalled, and underflow of the range at current lower than 3.5 mA.
3) For the marked format, exceeding of the range at voltage higher than 10.1 V is signalled.
4) For the marked format, exceeding of the range at voltage higher than 2.1 V is signalled.

Resolution of input data

Resolution means the smallest detectable change of the input variable expressed in technical units. It represents the value of the least significant bit of input data (LSB).

Tab. 5.2a. Resolution of input data of TC634 resistance temperature scanners

Resolution of input data of resistance temperature scanners

Scanner type	Data format			
	FS	Technical units		PID
		tenths of °C	tenths of Ω	
Pt100, W100 = 1.385	0.016021 °C/ LSB	0.1 °C/ LSB		
Pt100, W100 = 1.391	0.016021 °C/ LSB	0.1 °C/ LSB		
Ni1000, W100 = 1.617	0.0039673 °C/ LSB	0.1 °C/ LSB		
Ni1000, W100 = 1.500	0.0039673 °C/ LSB	0.1 °C/ LSB		
0 to 630 Ω	9.6131 mΩ/ LSB		0.1 Ω/ LSB	0.01 %/ LSB
0 to 2520 Ω	38.452 mΩ/ LSB		0.1 Ω/ LSB	0.01 %/ LSB

Tab. 5.2b Resolution of input data of TC634 current and voltage inputs

Resolution of input data of current and voltage inputs

Measurement range	Data format				
	FS	Technical units			PID
		μA	mV	tenths of mV	
0 to +20 mA	0.30518 μA	1 μA /LSB			0.01 % /LSB
+4 to +20 mA	0.24414 μA	1 μA /LSB			0.01 % /LSB
0 to +10 V	0.15259 mV		1 mV /LSB		0.01 % /LSB
0 to +2 V	0.030518 mV			0.1 mV /LSB	0.01 % /LSB

Tab. 5.3a. Accuracy of measurement of inputs for TC634 resistance temperature scanners

Accuracy of measurement of inputs for resistance temperature scanners

Scanner type	Maximum error (25 °C)	Temperature drift (0 to 50 °C)
Pt100, W100 = 1.385	±0.5 °C	±0.011 °C/ °C
Pt100, W100 = 1.391	±0.5 °C	±0.011 °C/ °C
Ni1000, W100 = 1.617	±0.4°C	±0.009 °C/ °C
Ni1000, W100 = 1.500	±0.4°C	±0.009 °C/ °C
0 to 630 Ω	±2 Ω	±40 mΩ/ °C
0 to 2520 Ω	±8 Ω	±70 mΩ/ °C

Tab. 5.3b Accuracy of measurement of TC634 current and voltage inputs

Accuracy of measurement of current and voltage inputs

Measurement range	Maximum error (25 °C)	Temperature drift (0 to 50 °C)
0 to +20 mA	±400 μA	±8 μA / °C
+4 to +20 mA	±400 μA	±8 μA / °C
0 to +10 V	±200 mV	±4 mV / °C
0 to +2 V	±40 mV	±800 μV / °C

5.2 Special Functions

Basic BM functions of TC603 to TC607 can be extended by special functions.

Special functions use standard-fitted inputs, or possibly PLC outputs, but their attendance requires more complex shell algorithms or complementation of the basic technical equipment of the input and output unit. These serving algorithms are realized by the system program, thus servicing performed by the user program remains simple.

Special functions are complemented to selected BM types per order (see Article 2.5). Always one special function may be complemented only.

5.2.1 Interrupt Inputs

Properties of interrupt inputs

Interrupt inputs allow for fast access to user programs for servicing of time critical operational states of the controlled object, and processing of fast changes of input signals processing of which by standard binary inputs is not possible.

Change of state of binary inputs DI0, DI1, DI2 or DI3 is done by the interruption process P42 which may be used to service the state. At the same time, flags are set determining source of the interrupt in the STAT state word. Activation of the interruption process from individual inputs can be controlled by setting the relevant bits of the CONT control word. In every input, it is possible to individually set the signal edge that activates the interrupt.

Interrupt inputs do not disturb neither limit basic functions of inputs DI0 to DI3 described under item 5.1.1.

Parameters of interrupt inputs

	TC601, TC602	TC603 to TC607
Number of interrupt inputs	-	4
Voltage for log. 0 (opening of the circuit)	max. 14V-, 13.5V~	
Voltage for log. 1 (closing of the circuit)	min. 18.5 V-, 17.5 V~ max. 30 V-, 30 V~	
Delay from log. 0 to log.1	max. 5 μs	
Delay from log. 1 to log.0	max. 5 μs	
Width of the input pulse	min. 30 μs	
Interrupt period	see item 10.5.8	
Response time of the PLC	see item 10.5.8	

For other parameters see item 5.1.1.

5.2.2 Counter of Type 3

Properties of the type 3 counter

Counter of type 3 is a unidirectional 16 bit counter of external events equipped with pre-selection, counting (CLK) and resetting input (RESET). The counter can operate as a freely running counter (in the range of 0 to 65535) or self-filling counter (in the range of 0 to pre-selection).

The binary input DI0 is used as the CLK input, binary input DI1 is used as the RESET input. When the RESET input state corresponds with log. 1 (closed input), the counter counts ascending edges of signals on the CLK input. When the RESET input state corresponds with log. 0 (open input), the counter is reset permanently. Overflow of the counter range or reaching of the pre-selection will evoke interruption process P44 of the user program. At the same time, setting of relevant bits in the STAT state word of the counter. Reset and blocking of the counter can be also done from within the user program by setting the relevant bit in the CONT control word of the counter.

Use of binary inputs as the counter inputs does not disturb neither limit their basic function described under item 5.1.1.

Parameters of the type 3 counter

	TC601, TC602	TC603 to TC607
Number of counters	-	1
Nominal voltage	24 V-	
Voltage for log. 0 (opening of the circuit)	max. 14 V-	
Voltage for log. 1 (closing of the circuit)	min. 18.5 V- max. 30 V-	
Range	16 bits (0 to 65535)	
Delay from log. 0 to log.1	max. 5 μs	
Delay from log. 1 to log.0	max. 5 μs	
Input frequency / resolution capability	max. 30 kHz / 3 pulses (10 kHz / 1 pulse)	
Interrupt period	min. 10 ms	
Pulse width	min. 30 μs	

For other parameters see item 5.1.1.

5.2.3 Admeasurement of Position by the Incremental Encoder

Incremental encoder admeasurement properties

The function of admeasurement by the incremental encoder is designed for processing of incremental encoder signals with outputs with an open collector.

In the admeasurement, it is operated with signed arithmetics in the range of long (4 bytes) between limits -2147483648 (8000 0000h) to +2147483647 (7FFF FFFFh) with 0 in between. It allows for admeasuring with resolution of the movement direction, setting of one pre-selection for every movement direction, resolution of position towards pre-selections and searching out of the reference point. After reaching of a pre-selection, overflow or underflow of the range, relevant bits are set in the STAT state word and the interruption process P44 is evoked. Control of admeasurement is performed through the CONT state word.

To connect the encoder, binary inputs DI0 (direct output of trace 1 of incremental encoder), DI1 (direct output of trace 2 of incremental encoder), and DI3 (direct output of the zero pulse of incremental encoder) are used.

Use of binary inputs for connection of incremental encoder does not disturb neither limit their basic function described under item 5.1.1.

Circuits parameters for incremental encoder connection

	TC601, TC602	TC603 to TC607
Number of encoders	-	1
Nominal voltage	24 V-	
Galvanic separation from other electric circuits	yes	
Voltage for log. 0 (opening of the circuit)	max. 14 V-	
Voltage for log. 1 (closing of the circuit)	min. 18.5 V- max. 30 V-	
Current for log. 1	typ. 10 mA	
Delay from log. 0 to log.1	max. 5 μs	
Delay from log. 1 to log.0	max. 5 μs	
Input frequency / resolution capability	max. 30 kHz / 12 pulses (2.5 kHz / 1 pulse)	
Pulse width	min. 30 μs	
Interrupt period	min. 10 ms	
Range of the admeasured variable	32 bits (- 2 147 483 648 to + 2 147 483 647)	

For other parameters see item 5.1.1.

5.2.4 Measurement of the Signals Period and Phase Shift

Properties of the function

The function allows for measurement of the signal period at the BM input DI0 or measurement of the phase shift of two signals at BM inputs DI0 and DI1.

Measured values express the number of cycles of the internal clock signal between two descending edges of the measured signal (measured signals). By converting the values in the user program, it is possible to obtain values in time units. Time of the cycle of the internal clock signal is 30.5175 μs.

Use of binary inputs for measurement of the period or phase shift does not disturb neither limit their basic function described in Article 5.1.1.

Parameters of measurement circuits

	TC601, TC602	TC603 to TC607
Possibility of function complementation	-	yes
Nominal voltage	24 V-	
Voltage for log. 0 (opening of the circuit)	max. 14 V-	
Voltage for log. 1 (closing of the circuit)	min. 18.5 V- max. 30 V-	
Delay of input from log. 0 to log.1	max. 5 μs	
Delay of input from log. 1 to log.0	max. 5 μs	
Input frequency	1 Hz to 1 kHz	
Pulse width	min. 30 μs	

For other parameters see Article 5.1.1.

6. Packaging

Individual BM's and EM's are packaged together with instructions according to the internal packaging regulation into boxes provided with a fixing insert. Outside packaging is realized according to the order extent and way of transport, in a transport cover provided with transport tags and other data necessary for the transport.

7. Transport

Transport from the producer is performed in a way agreed upon at ordering of the product. Transport via the customer's own means must be performed using roofed transport means, in a position given on the tag present on the cover. The box must be stored in such a way so that no unprompted movement and damage of the outside cover can occur. The product must not be exposed to direct effect of weather conditions in the course of the transportation. The transport may be realized under temperatures -25 °C to 70 °C, relative humidity of 5 % to 95 % (non-condensing), and pressure >70 kPa.

8. Storage

Storage of the product is allowed only in clean areas without conductive dust, aggressive gases and vapours, under temperatures of -25 °C to 70 °C, relative humidity 5%, and pressure >70 kPa. At storage, sudden changes in temperature neither formation of dew on the product may occur. Long-term storage of the product under temperatures close to the upper limit of the allowed temperature reduces capacity of the backing battery. Most suitable storage temperature is 20 °C.

9. Installation

9.1 Principles of Proper Installation

Tecomat PLC's of the TC600 series are built-in devices designed for being mounted in closed cases. From the viewpoint of correct function of the system, it is necessary to choose the size and design of the case so that by the construction arrangement, it is possible to limit as much as possible the effect of especially power parts of the device on the PLC. Limitation of the disturbing effect can be achieved by suitable dislocation of parts of the equipment, by their proper interconnection and elimination of inductive loads.

In general the following principles apply:

- from the viewpoint of disturbances and cooling, it is more suitable to use a metal case than a plastic one
- the PLC should be place if possible in an area spatially separated from powerful closing elements of the controlled technology
- conductors should be laid in cable troughs on a defined basis, formation of bights should be prevented
- parallel running of conductors of the power supply, analog signals, PLC inputs and outputs with conductors of the power alternating part of the distribution should not be realized unnecessarily
- shielding of leading-in cables of analog inputs and outputs should be connected with the frame by the shortest connection possible, formed directly by the shielding plied apart
- cover of modules (a protective connector) should be connected as close as possible with the non-live part of the case or by the shortest possible independent connection with the protective connector of the case, the connection should be realized by a conductor with the minimum cross section of 2.5 mm^2

- inductive loads should be serviced in the place of origination of the disturbance

Principle of various ways of servicing the inductive load, aids for the design of RC disturbances elimination elements, overview of sets of disturbances elimination elements supplied by the PLC producer and other recommendations are given in the handbook *Design of Tecomat Programmable Logic Controllers, TXV 001 08.01.*

9.2 Ensuring of the Required Operational Temperature

In cases without forced inside air circulation, the PLC must be placed in such a way so that the distance between the bottom and top side of the PLC and inside sides of the case is at least 100 mm. If this cannot be ensured by good unprompted air circulation, it is necessary to ensure air circulation by building in a ventilator. The maximum allowed air temperature entering the regulator is 55 °C. The PLC itself participates in the output losses by the maximum of 13 W (20 VA) of the power input, typically the loss of 0.25 W at every closed binary input and 0.2 W at every closed transistor output. Losses at closed relay outputs are included the PLC power input.

9.3 The Mounting

The PLC is mounted in vertical position on the U bar, ČSN EN 50022 (idt EN 50022:1977). Outside proportions of the PLC BM, EM and EM/2 are apparent from Figs. 9.1, 9.2 and 9.3.

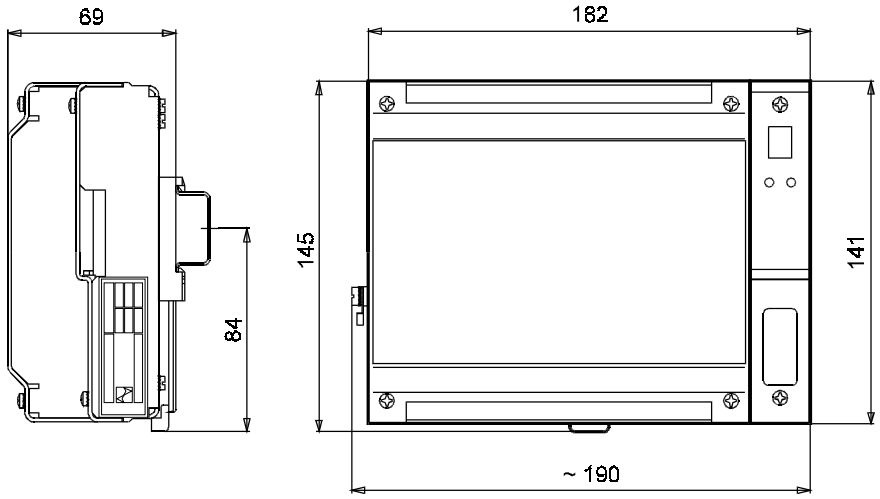


Fig. 9.1 Mechanic proportions of PLC BM of the TC600 series

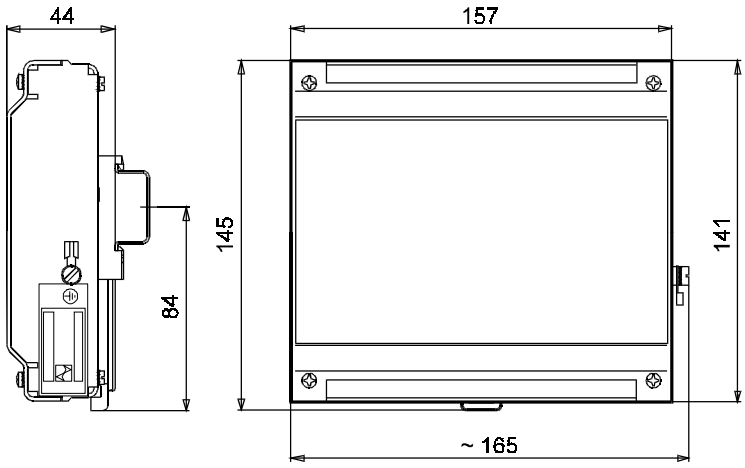


Fig. 9.2 Mechanic proportions of PLC EM of the TC600 series

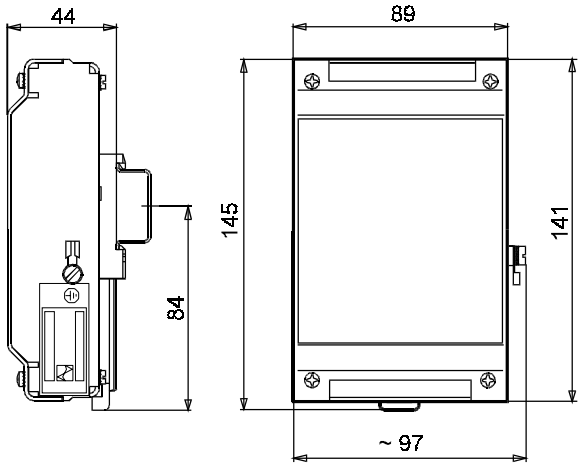


Fig. 9.3 Mechanic proportions of PLC EM/2 of the TC600 series

EM and EM/2 are placed always on the right side from the BM. EM (EM/2) are connected mutually as well as with the BM by a band cable which is part of the EM (EM/2). Cable socket is connected into a socket plug on the right side of the BM (EM/2). After connecting the cable, modules on the bar are moved to their close proximity. Possible ways of extension are given in Figs. 9.4 to 9.7.

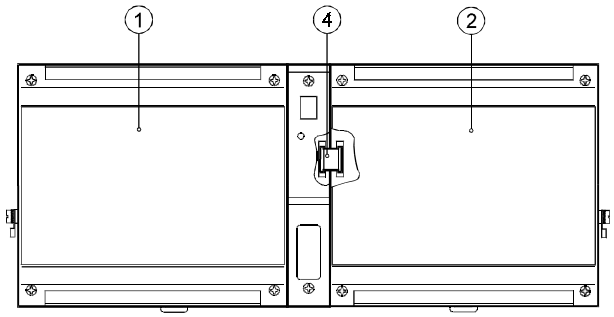


Fig. 9.4 BM extension by one EM

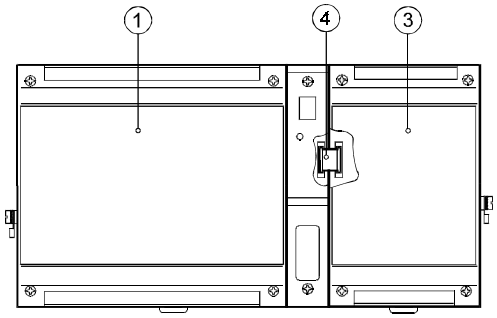


Fig. 9.5 BM extension by one EM/2

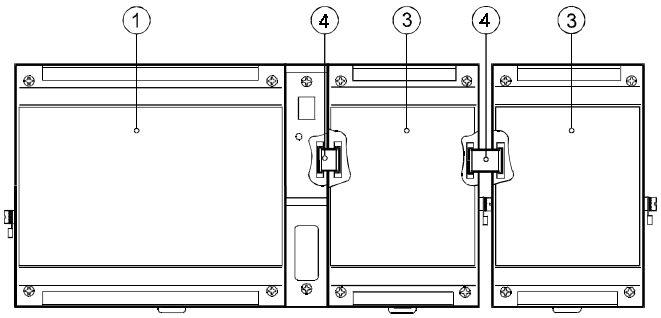


Fig. 9.6 BM extension by two EM/2

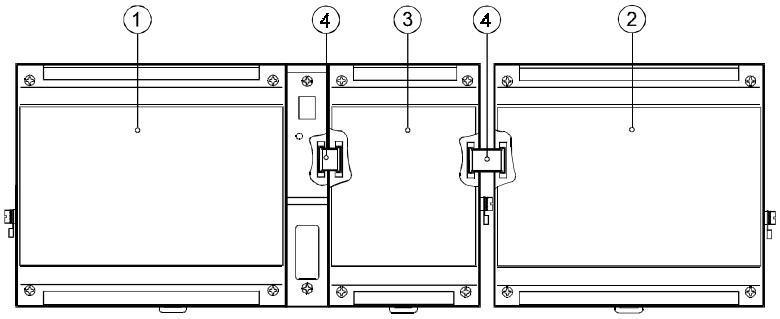
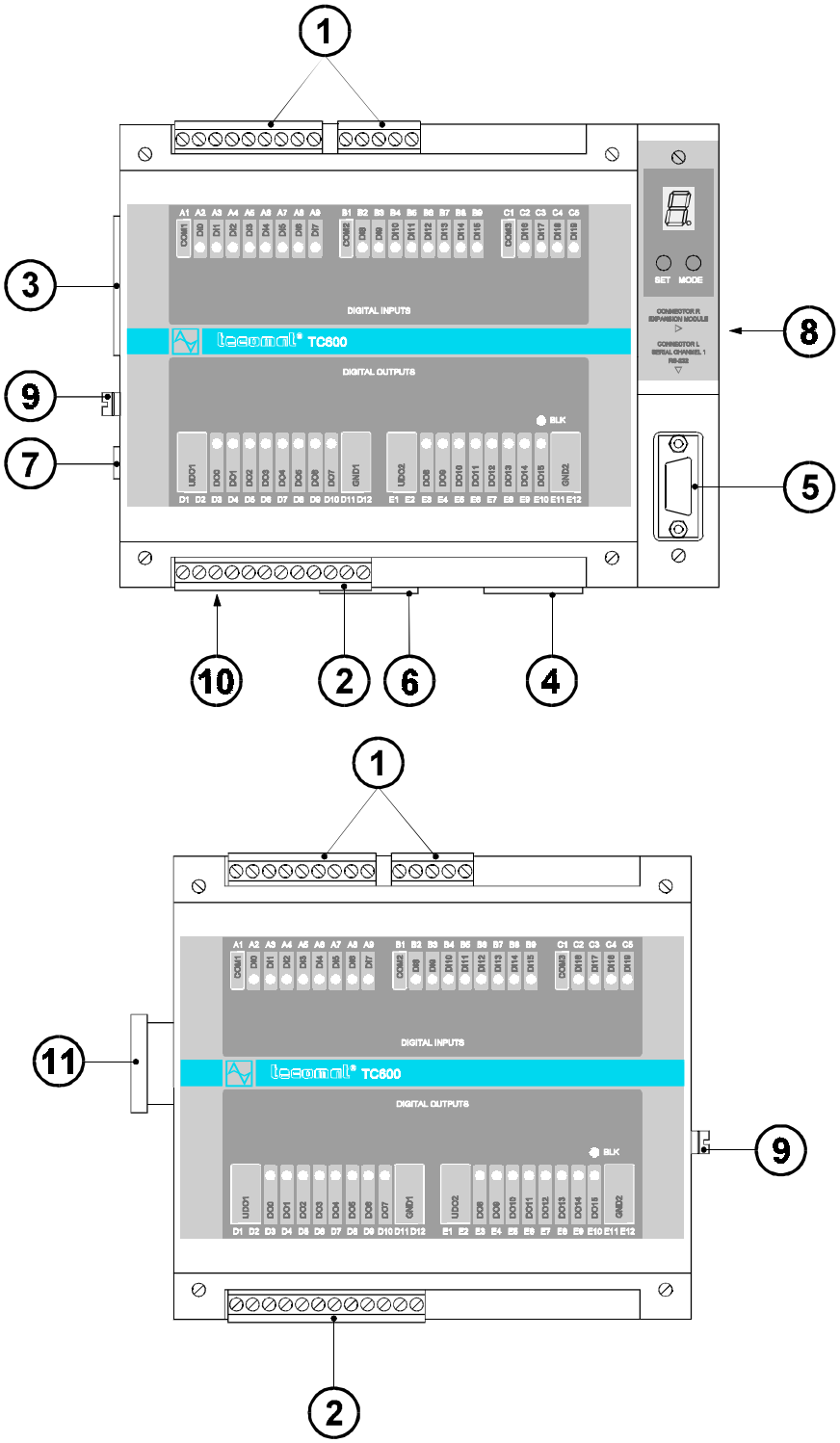


Fig. 9.7 BM extension by one EM/2 and one EM

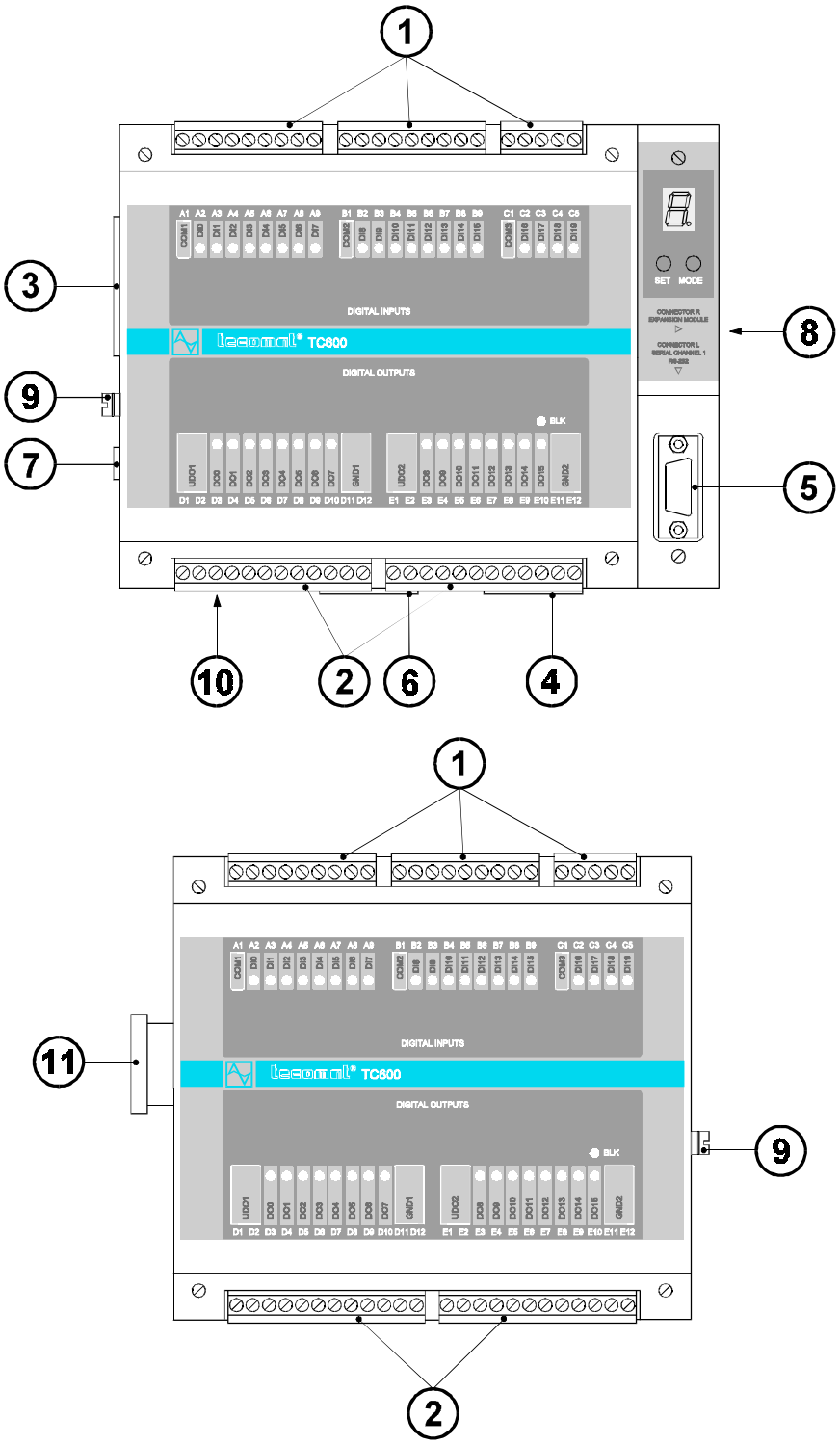
1 - Basic module (BM)
2 - Extension module (EM)
3 - Half extension module (EM/2)
4 - Connection cable

9.4 Arrangement of Connecting of Terminal Boards



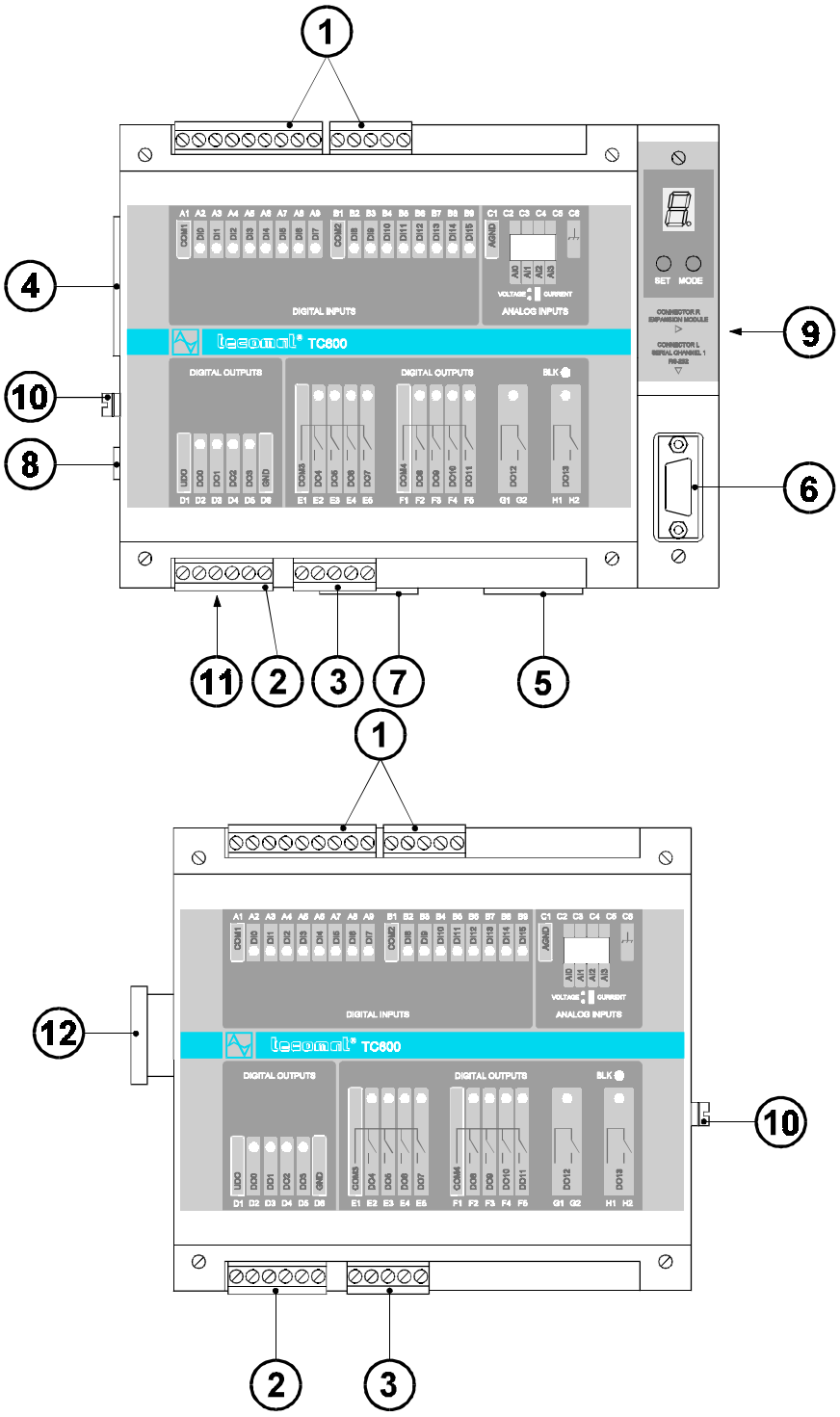
1 terminal boards **A, B** of binary inputs
2 terminal board **D** of binary transistor outputs
3 terminal board **P** of optional analog outputs or CH3
4 terminal board **K** of optional CH1 interface
5 socket **L** of CH1 interface RS-232
6 terminal board **N** of optional CH2 interface
7 terminal board **M** of the PLC power supply
8 socket plug **R** for connection of the EM
9 connector for connection of the protective conductor
10 fuse of the power supply converter
11 socket for connection to the BM

Fig. 9.8 Arrangement of Connecting Terminal Boards of TC601 BM and TC621 EM (below)



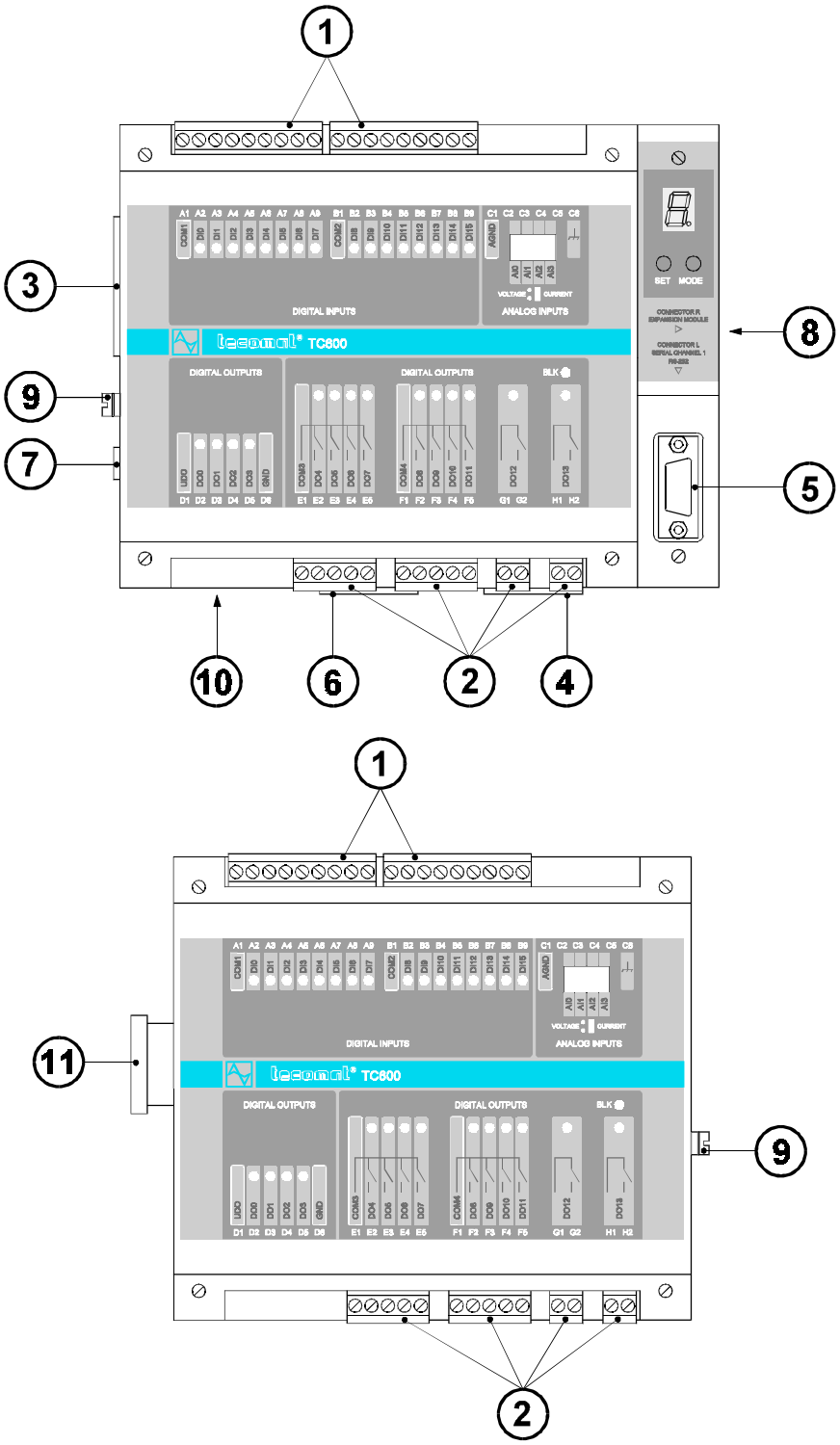
1 terminal boards **A, B, C** of binary inputs
2 terminal board**s D, E** of binary transistor outputs
3 terminal board **P** of optional analog outputs or CH3
4 terminal board **K** of optional CH1 interface
5 socket **L** of CH1 interface RS-232
6 terminal board **N** of optional CH2 interface
7 terminal board **M** of the PLC power supply
8 socket plug **R** for connection of the EM
9 connector for connection of the protective conductor
10 fuse of the power supply converter
11 socket for connection to the BM

Fig. 9.9 Arrangement of Connecting Terminal Boards of TC602 BM (above) and TC622 EM (below)



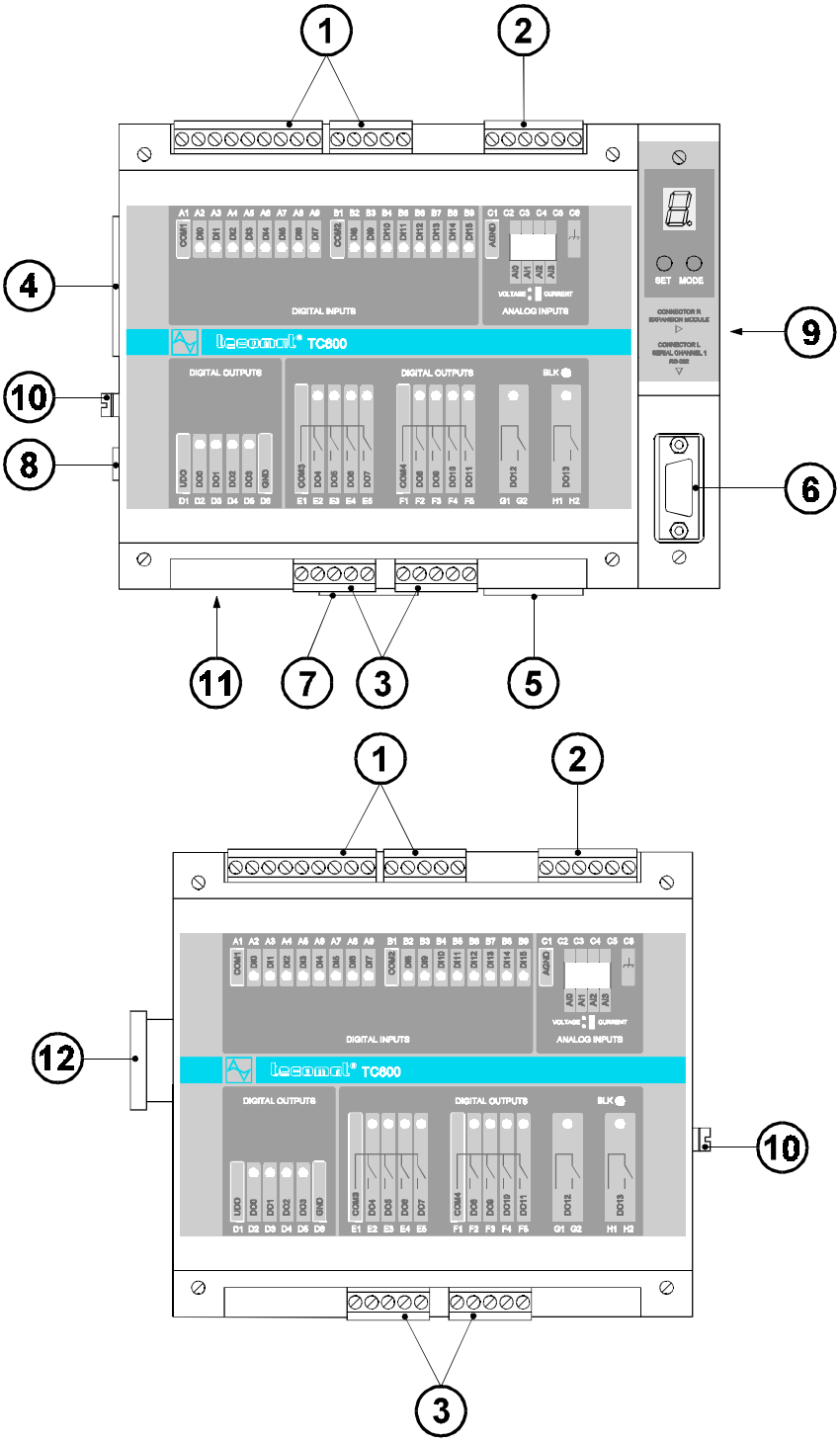
1 terminal boards **A, B** of binary inputs
2 terminal board **D** of binary transistor outputs
3 terminal board **E** of binary relay outputs
4 terminal board **P** of optional analog outputs or CH3
5 terminal board **K** of optional CH1 interface
6 socket **L** of CH1 interface RS-232
7 terminal board **N** of optional CH2 interface
8 terminal board **M** of the PLC power supply
9 socket plug **R** for connection of the EM
10 connector for connection of the protective conductor
11 fuse of the power supply converter
12 socket for connection to the BM

Fig. 9.10 Arrangement of Connection Terminal Boards of TC603 BM (above) and TC623 EM (below)



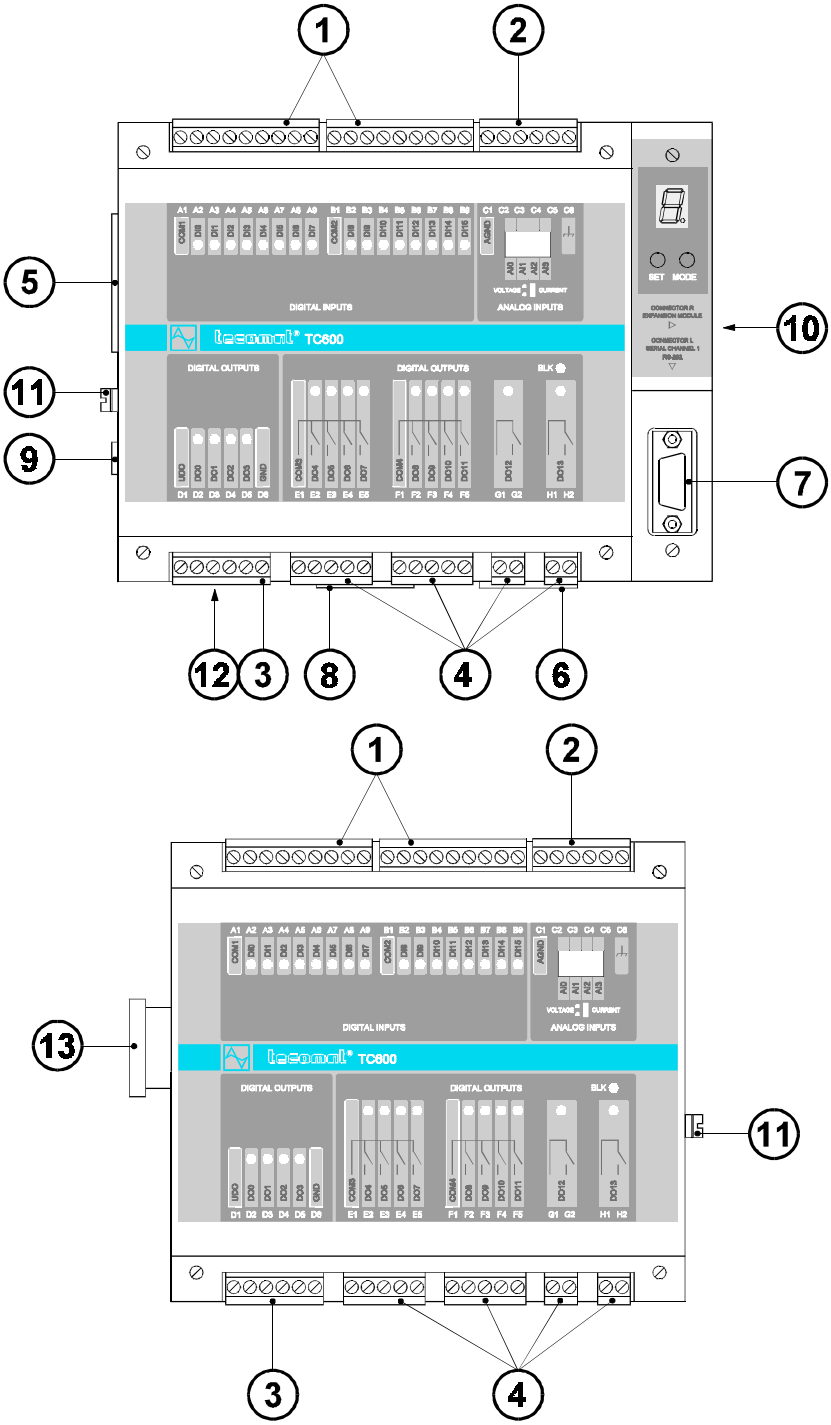
1 terminal boards **A, B** of binary inputs
2 terminal boards **E, F, G, H** of binary relay outputs
3 terminal board **P** of optional analog outputs or CH3
4 terminal board **K** of optional CH1 interface
5 socket **L** of CH1 interface RS-232
6 terminal board **N** of optional CH2 interface
7 terminal board **M** of the PLC power supply
8 socket plug **R** for connection of the EM
9 connector for connection of the protective conductor
10 fuse of the power supply converter
11 socket for connection to the BM

Fig. 9.11 Arrangement of Connection Terminal Boards of TC604 BM (above) and TC624 EM (below)



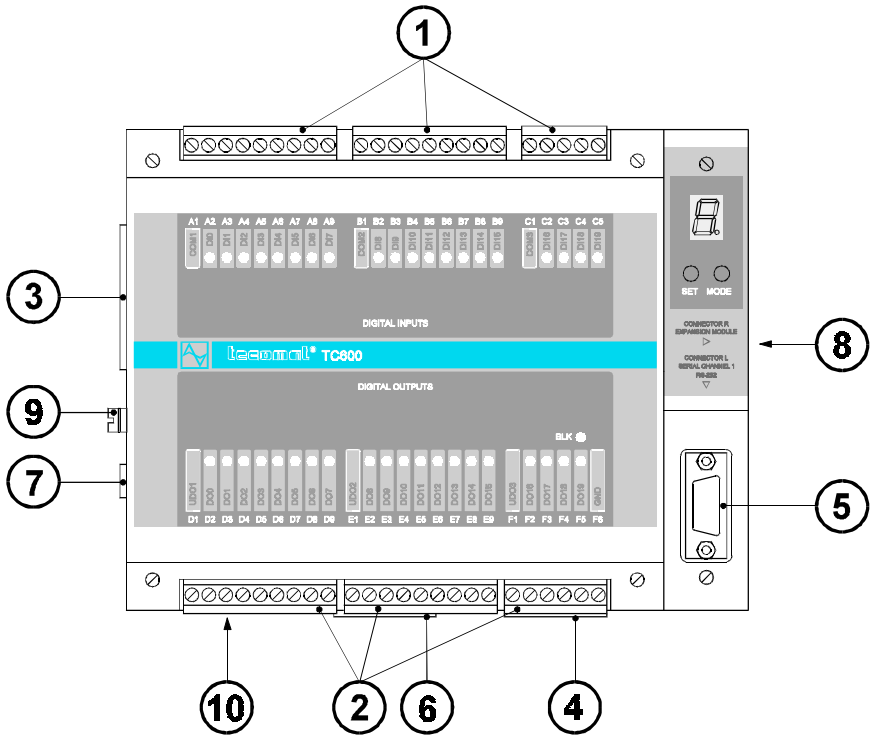
1 terminal boards **A, B** of binary inputs
2 terminal board **C** of analog inputs
3 terminal boards **E, F** of binary relay outputs
4 terminal board **P** of optional analog outputs or CH3
5 terminal board **K** of optional CH1 interface
6 socket **L** of CH1 interface RS-232
7 terminal board **N** of optional CH2 interface
8 terminal board **M** of the PLC power supply
9 socket plug **R** for connection of the EM
10 connector for connection of the protective conductor
11 fuse of the power supply converter
12 socket for connection to the BM

Fig. 9.12 Arrangement of Connection Terminal Boards of TC605 BM (above) and TC625 EM (below)



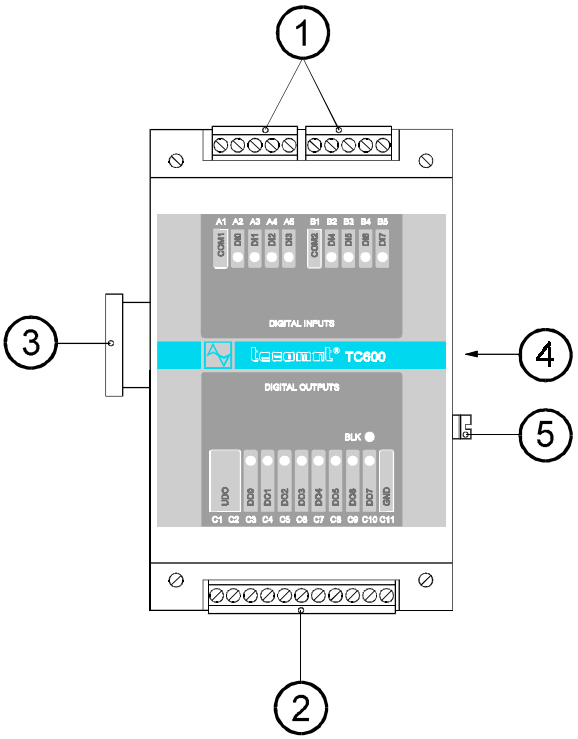
1 terminal boards **A, B** of binary inputs
2 terminal board **C** of analog inputs
3 terminal board **D** of binary transistor outputs
4 terminal boards **E, F, G, H** of binary relay outputs
5 terminal board **P** of optional analog outputs of CH3
6 terminal board **K** of optional CH1 interface
7 socket **L** of CH1 interface RS-232
8 terminal board **N** of optional CH2 interface
9 terminal board **M** of the PLC power supply
10 terminal board **R** for connection of the EM
11 connector for connection of the protective conductor
12 fuse of the power supply converter
13 socket for connection to the BM

Fig. 9.13 Arrangement of Connection Terminal Boards of TC606 BM (above) and TC626 (below)



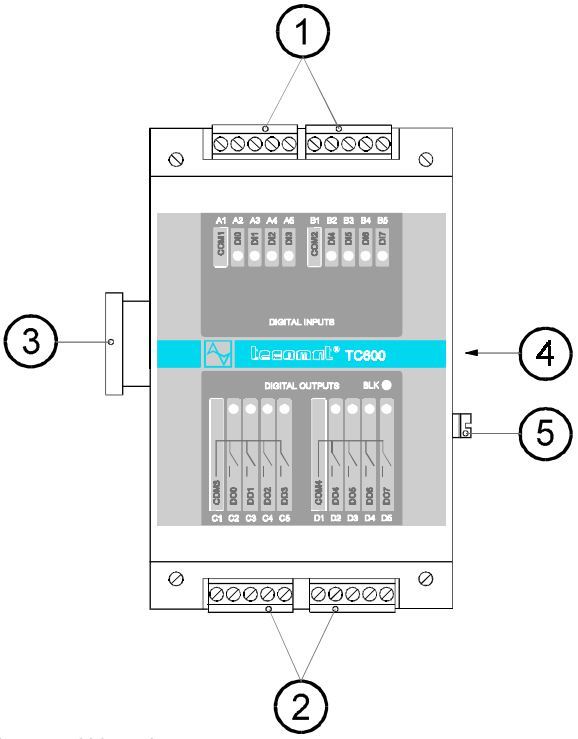
1 terminal boards **A, B, C** of binary inputs
2 terminal boards **D, E, F** of binary transistor outputs
3 terminal board **P** of optional analog outputs or CH3
4 terminal board **K** of optional CH1 interface
5 socket **L** of CH1 interface RS-232
6 terminal board **N** of optional CH2 interface
7 terminal board **M** of the PLC power supply
8 socket plug **R** for connection of the EM
9 connector for connection of the protective conductor
10 fuse of the power supply converter

Fig. 9.14 Arrangement of Connection Terminal Boards of TC607 BM



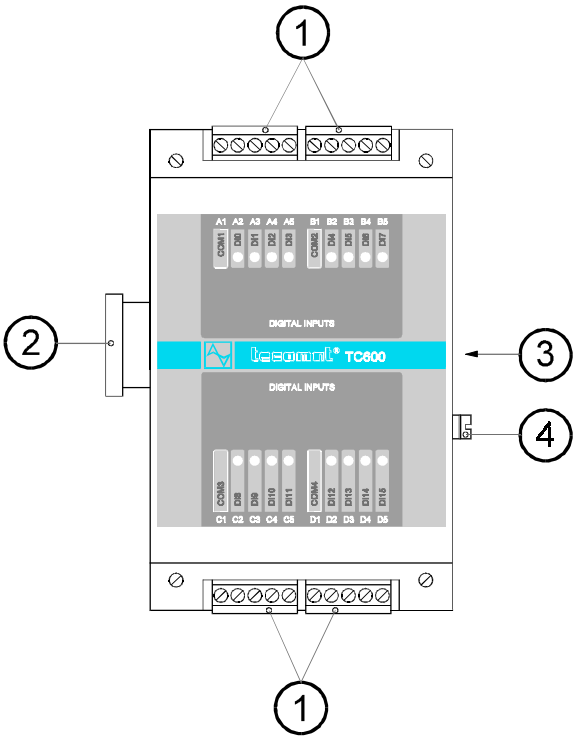
1 terminal boards **A, B** of binary inputs
2 terminal board **C** of binary transistor outputs
3 socket for connection to the BM
4 socket plug for connection of the EM or EM/2
5 connector for connection of the protective conductor

Fig. 9.15 Arrangement of Connection Terminal Boards of TC631 EM/2



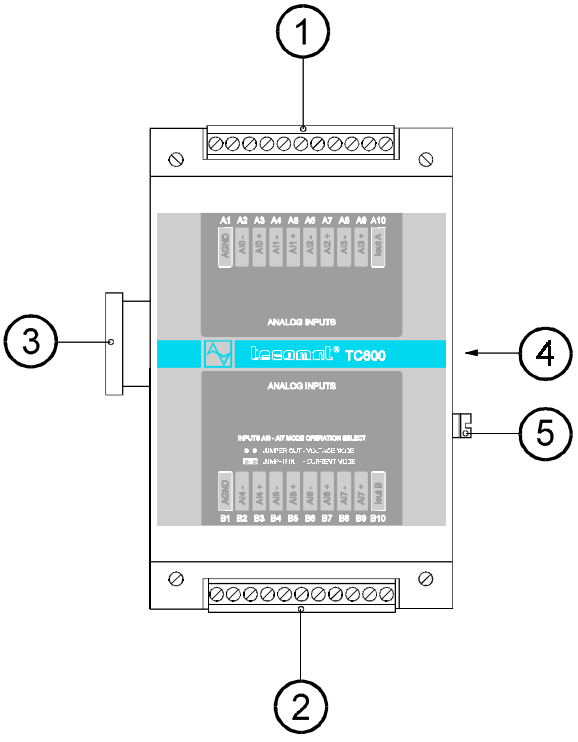
1 terminal boards **A, B** of binary inputs
2 terminal board **C** of binary relay outputs
3 socket for connection to the BM
4 socket plug for connection of the EM or EM/2
5 connector for connection of the protective conductor

Fig. 9.16 Arrangement of Connection Terminal Boards of TC632 EM/2



1 terminal boards **A, B, C, D** of binary inputs
2 socket for connection to the BM
3 socket plug for connection of the EM or EM/2
4 connector for connection of the protective conductor

Fig. 9.17 Arrangement of Connection Terminal Boards of TC633 EM/2



1 terminal board **A** of analog inputs AI0 to AI3
2 terminal board **B** of analog inputs AI4 to AI7
3 socket for connection to the BM
4 socket plug for connection of the EM or EM/2
5 connector for connection of the protective conductor

Fig. 9.18 Arrangement of Connection Terminal Boards of TC634 EM

9.5 Connection of the PLC Inputs and Outputs

With the exception of the protective grounding connector and the CH1 RS-232 interface, PLC inputs and outputs are connected using removable terminal boards which are inserted into the appropriate socket plugs of inputs and outputs. The screw part of the terminal board is constructed for connection of a full conductor with cross section up to 1.5 mm^2 or a wire with cross section up to 1 mm^2. The minimum recommended cross section of the full conductor is 0.2 mm^2, of the wire 0.5 mm^2. Terminal boards are a part of the PLC additional package.

Connection terminal boards are not protected against exchange by any coding element, check the connection before putting them into operation!

9.5.1 Connection of the Protective Connector

The PLC protective connector must be interconnected with the inside protective connector of the case. Interconnection must meet requirements of ČSN 33 2000-5-54 (mod IEC 364-5-54:1980). From the viewpoint of disturbances, in cases with the metal mounting board it is suitable to connect the protective terminal board with the mounting board by the shortest connection possible. The protective connector is marked with the label 417-IEC-5019-a  .

9.5.2 PLC Power Supply

Power supply of the PLC, input and output circuits, must be in the overvoltage category II according to ČSN 33 0420 (eqv IEC 664:1980, IEC 664A:1981).

The power supply must meet conditions of the SELV supply according to ČSN 33 2000-4-41 (mod IEC 364-4-41:1992).

Between the primary and secondary winding of the transformer, a Cu shielding foil must be wound up, connected with the inside protective terminal board of the case or the winding must be arranged spatially in such a way so that the mutual capacity between the windings is minimized. It is suitable to insert switches into the supply lead which make work on program debugging, maintenance and possible repairs easier.

The power supply voltage of the PLC, 24 V~ ±20%, 50 - 60 Hz ±5% or 24 V- ±20 %, is connected to connectors M1 and M2 of the terminal board marked as POWER INPUT. In connection of the direct-current supply, voltage polarity does not matter. Permanent exceeding of the tolerance upper limit may cause breaking of the voltage protective element of the PLC converter. For dimensioning of the supply, it is necessary to consider the maximum input of 13 W (20 VA), which also contains input of coils of the relay of binary relay outputs.

PLC power supply can also be used for supplying of binary inputs

Switches of input circuits may be supplied from the same power supply as the BM internal converter. Input of the closed binary input is typically 0.25 W (0.25 VA). For connection of the binary inputs supply see item 9.5.3.

Circuits closed by binary outputs must be supplied from an independent power supply or at least from an independent transformer winding. The supply must be dimensioned according to the concrete input of the loads. Input of the output transistor circuit is typically 0.2 W for current of 1 A. For connection of the binary outputs power supply see items 9.5.4 and 9.5.5.

9.5.3 Connection of Binary Inputs

PLC binary inputs are led out to connectors of terminal boards marked as DIGITAL INPUTS. Input switches are connected between the input connector and the common connector of the group. In Fig. 9.17, scheme of connection of switches and the power supply to one group of inputs of TC601 to TC607 (TC621 to TC626) is indicated.

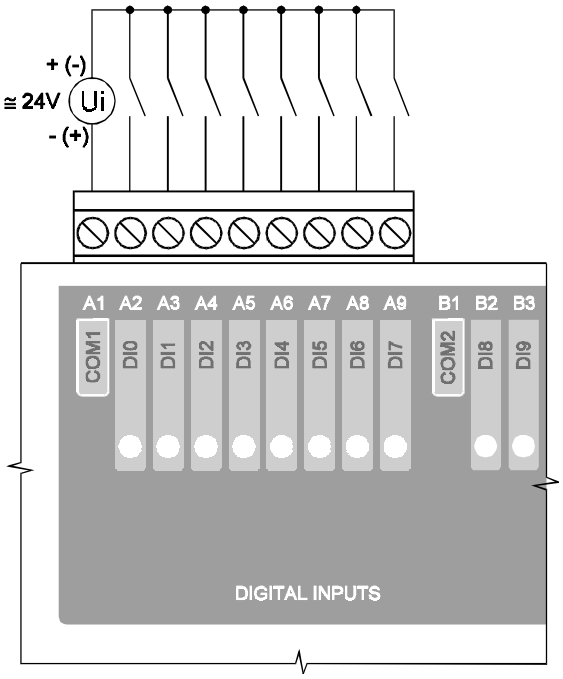


Fig. 9.17 Example of connection of switches to binary inputs of the PLC of the TC600 series

Supply voltage of a group of switches may be connected in arbitrary polarity, within the group individual inputs must be poled identically.

For fitting and marking of terminal boards of binary inputs of individual PLC types see Article 9.4.

9.5.4 Connection of Binary Transistor Outputs

Transistor switches of binary outputs are led out to connectors of terminal boards marked as DIGITAL OUTPUTS. In Fig. 9.18, scheme of connection of loads and the power supply to one of the groups of outputs of TC601 (TC621), TC602 (TC622) is indicated. Transistor outputs of other types of the series are connected in the similar way as well.

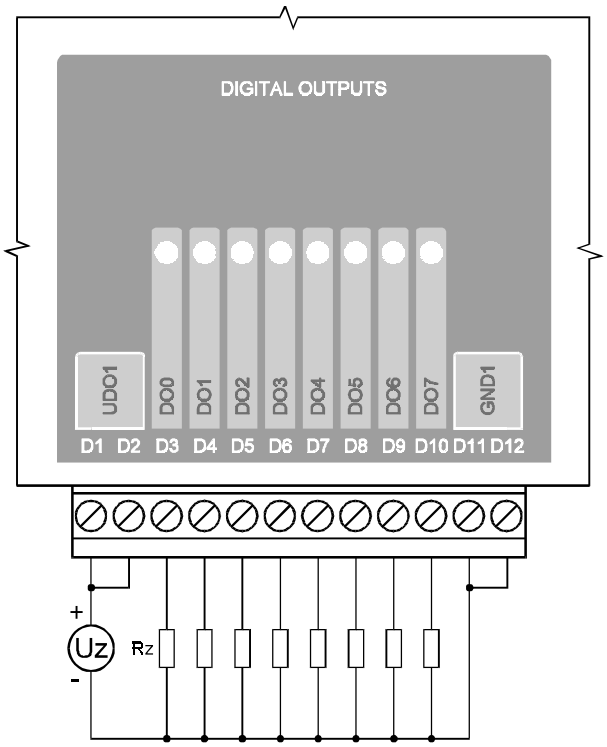


Fig. 9.18 Example of connection of loads to binary transistor outputs of the PLC of the TC600 series

For fitting and marking of terminal boards of binary transistor outputs of individual PLC types see Article 9.4.

9.5.5 Connection of Binary Relay Outputs

Contacts of the relay of binary outputs are led out to terminal boards marked as DIGITAL OUTPUTS. Fig. 9.19 shows scheme of connection of loads to relay contacts led out to the terminal board in the group, and of independently led out contact of TC604 (TC624), TC606 (TC626). Relay outputs of other types of the series are connected similarly.

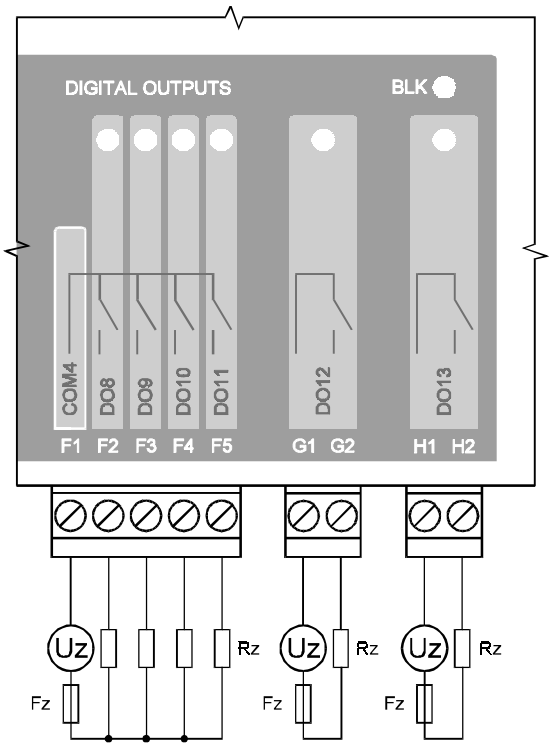


Fig. 9.19 Example of connection of loads to binary relay outputs of the PLC of TC600 series

For fitting and marking of terminal boards of binary relay outputs of individual PLC types see Article 9.4.

9.5.6 Connection of Analog Inputs of TC605, TC606, TC625, TC626

Analog inputs are led out to connectors of the terminal board marked as ANALOG INPUTS. In Fig. 9.20, scheme of connection of current and voltage signal supplies to analog inputs of TC605 (TC625), TC606 (TC626) is indicated.

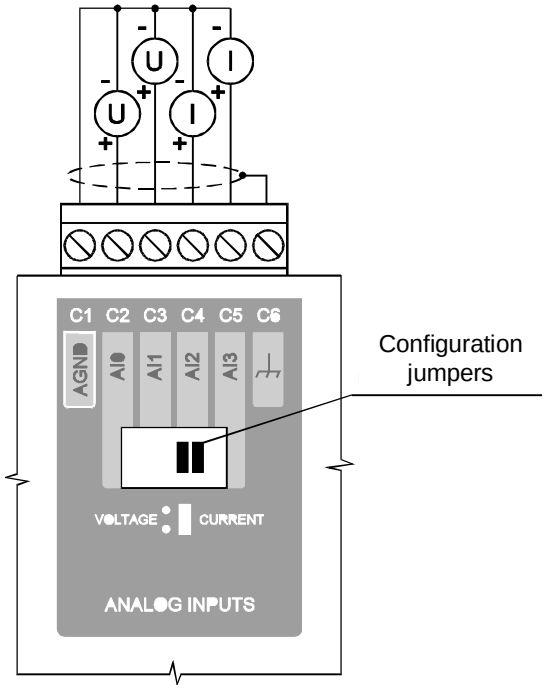


Fig. 9.20 Example of connection of current and voltage signals to analog inputs of the PLC of the TC600 series

Type of the analog input is set by a jumper

Connection of a relevant jumper modifying the voltage input to the current one, must correspond with the current signal supply connected to the input. Disconnected jumper corresponds with the voltage input, connected jumper corresponds with the current input. Jumpers are accessible through openings in the regulator cover. Setting of jumpers for the required input type is shown on the label close to the jumpers.

Connector C6 connected with the controller cover, is intended for connection of the shielding of lead in conductors. If the shielding is connected with the device frame in another place, for example to the input terminal board of the distribution board, it is no more connected with the C6 connector. Examples of the installation realization in the distribution board are contained in the handbook *Design of Tecomat Programmable Logic Controllers, TXV 001 08.01.*

For fitting of terminal boards of analog inputs of individual PLC types see Article 9.4.

9.5.7 Connection of TC634 Analog Inputs

Analog inputs of the TC634 module and the internal current supply are led out to terminal boards marked as ANALOG INPUTS. Fig. 9.21 shows scheme of connection of current and voltage signal supplies to analog inputs AI0-AI3, Fig. 9.22 shows scheme of connection of resistance temperature scanners to inputs AI4-AI7.

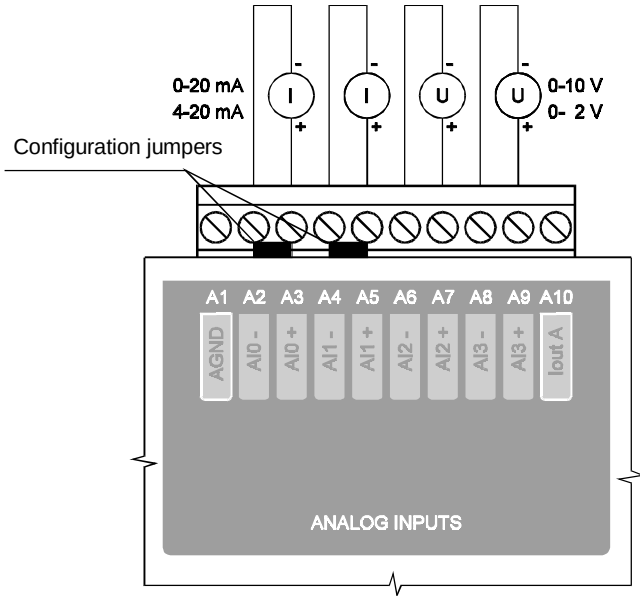


Fig. 9.21 Example of connection of current and voltage signals to the TC634 analog inputs

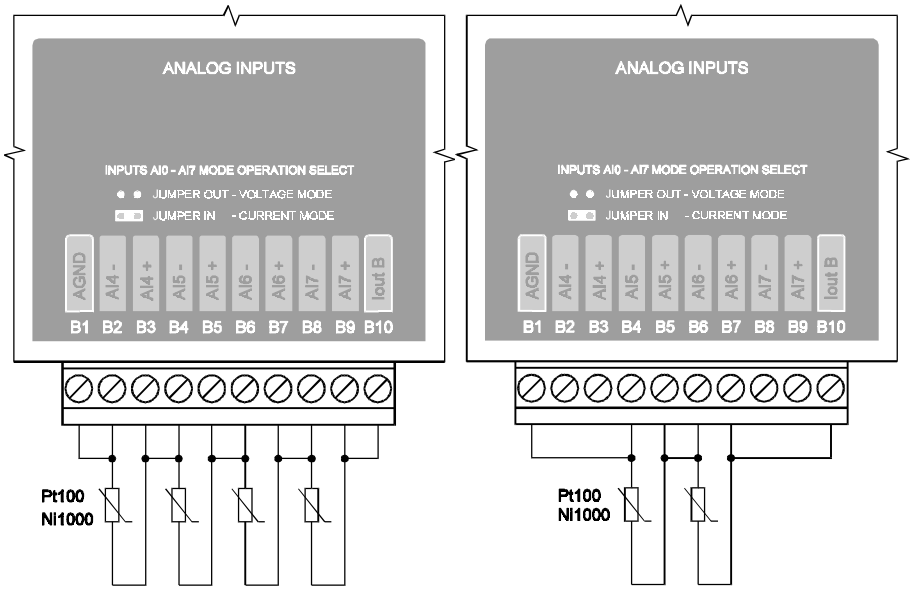


Fig. 9.22 Example of connection of resistance temperature scanners to the TC634 analog inputs

Type of the analog input is set by a jumper

Every input must be set individually by the jumper for the direct-current voltage or current signal supply. Jumpers are placed above corresponding couples of input connectors, and are accessible through openings in the controller cover. Disconnected jumper corresponds with the voltage input, connected jumper corresponds with the current input. For passive resistance temperature scanners, voltage input type is set (the jumper is disconnected).

9.5.8 Connection of Analog Outputs

Optionally fitted BM analog outputs of TC601 to TC607 are led out to connectors P1 to P10 of the terminal board marked as OPTIONAL I/O.

Lead out of analog outputs of the OT-13 piggyback

Connector	Signal	Note
P1	AO0	analog output 0
P3	AO1	analog output 1
P5	AO2	analog output 2
P7	AO3	analog output 3
P2, P4, P6, P8, P9, P10	AGND	common analog ground

In Fig. 9.23, scheme of connection of loads to the OT-13 piggyback analog outputs is indicated.

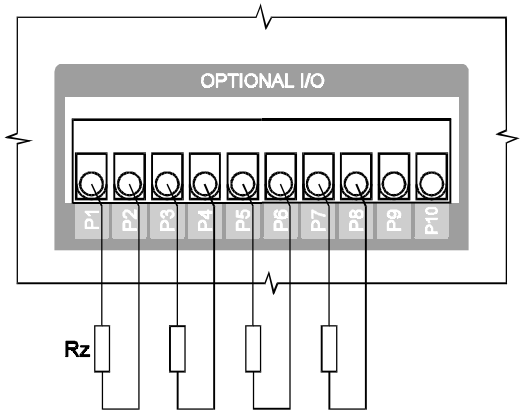


Fig. 9.23 Connection of loads to the OT-13 piggyback analog outputs

Lead out of analog outputs of the OT-14 piggyback

Connector	Signal	Note
P1	AO0	analog output 0
P2	AO4	analog output 4
P3	AO1	analog output 1
P4	AO5	analog output 5
P5	AO2	analog output 2
P6	AO6	analog output 6
P7	AO3	analog output 3
P8	AO7	analog output 7
P9, P10	AGND	common analog ground

In Fig. 9.24, scheme of connection of loads to the OT-14 piggyback analog outputs is indicated.

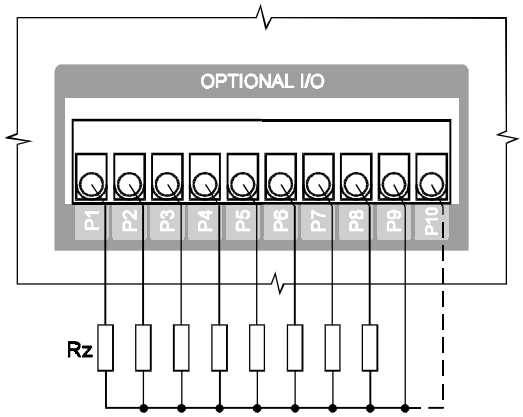


Fig. 9.24 Connection of loads to the OT-14 piggyback analog outputs

Examples of the installation realization in the distribution board are contained in the handbook *Design of Tecomat Programmable Logic Controllers, TXV 001 08.02.*

For fitting of terminal boards of analog outputs of individual PLC types see Article 9.4.

9.5.9 Connection of the CH1 Interface

CH1 RS-232 interface

Interface RS-232 of CH1 is designed especially for connection of a computer of the PC class performing the function of a programming device. Binding circuits of the interface are led out to the 9-pole socket Dsub (CONNECTOR L) marked as SERIAL CHANNEL 1/RS-232. The connection is realized by the cable TXK 646 51.06 ended on the PC side by the 9-pole Dsub socket.

If the optional CH1 interface is fitted, by connecting the cable TXK 646 51.06, signals of CH1 will be disconnected automatically from the optional interface.

Signals of the CH1 RS-232 interface

Lead out	Signal	Signal type	Use
L2	RxD	input	data signal
L3	TxD	output	data signal
L5	GND	signal ground	
L7	RTS	output	controlling signal [1)]
L8	CTS	input	controlling signal [1)]
L9	232DIS	input	CH1 interface switch

[1)] Use of the signal is described in the handbook *Serial Communication of Tecomat Programmable Logic Controllers, TXV 001 06.01.* Still level of the signal corresponds with the value of logical 1.

Optional CH1 RS-485 interface

Binding circuits of the interface are led out to connectors K1 to K6 of the terminal board marked as SERIAL CHANNEL 1.

Lead out of binding circuits of piggybacks MR-04, MR-09 of CH1

Connector	Signal	Signal type	Use
K1		frame	connection of the shielding
K2, K4	RxD-/TxD-	input/output	data signal
K3, K5	RxD+/TxD+	input/output	data signal
K6	GND	signal ground	

Interconnection is realized by a couple of twisted shielded conductors. In general, it holds that for higher communication speeds and greater lengths of cables, it is necessary to use higher cross section of conductors. For reduction of reflections, the line is impedance-adjusted by terminators on both ends of the line. In some cases, it is necessary to interconnect signal grounds to balance their potentials. In Fig. 9.25, scheme of interconnection of the RS-485 interface at the marginal and internal equipment of the network is indicated.

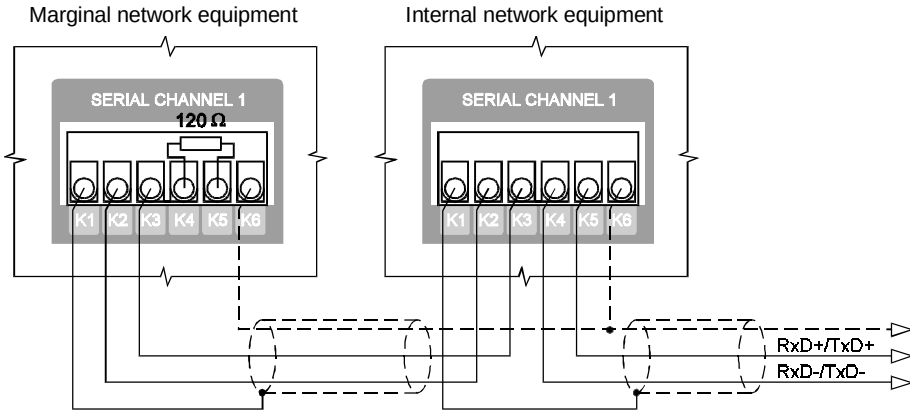


Fig. 9.25 Interconnection of two CH1 interfaces RS-485 of the PLC of TC600 series

Optional CH1 RS-422 interface

Binding circuits of the interface are led out to connectors K1 to K6 of the terminal board marked as SERIAL CHANNEL 1.

Lead out of binding circuits of the piggyback MR-17 of CH1

Connector	Signal	Signal type	Use
K1		frame	connection of the shielding
K2	TxD-	output	data signal
K3	TxD+	output	data signal
K4	RxD-	input	data signal
K5	RxD+	input	data signal
K6	GND	signal ground	

Interconnection is realized by two couples of shielded twisted conductors. In general, it holds that for higher communication speeds and greater lengths of cables, it is necessary to use greater cross section of the conductors. For reduction of reflections, the line is impedance-adjusted by terminators on the side of the receivers. In some cases, it is necessary to interconnect the signal grounds to balance the potentials. In Fig. 9.26, scheme of interconnection of two RS-422 interfaces is indicated.

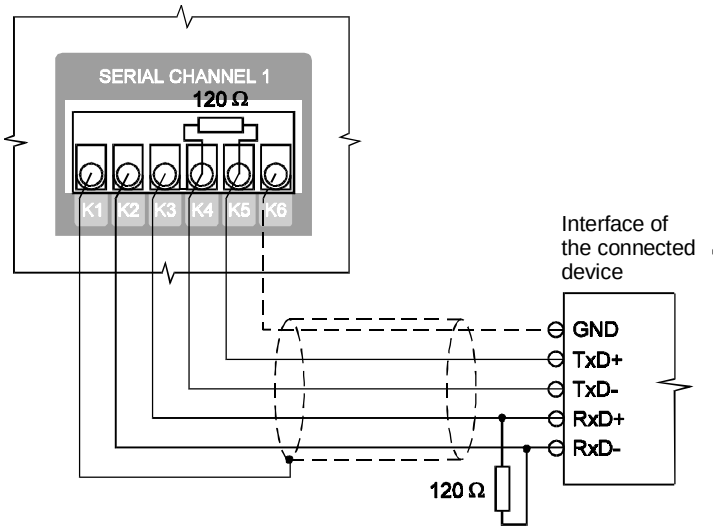


Fig. 9.26 Interconnection of CH1 interfaces RS-422 of the PLC of TC600 series

9.5.10 Connection of the CH2 Interface

Optional CH2 RS-232 interface

Binding circuits of the interface are led out to connectors N1 to N6 of the terminal board marked as SERIAL CHANNEL 2.

Lead out of binding circuits of the piggyback MR-02 of CH2

Lead out	Signal	Signal type	Use
N1		frame	connection of the shielding
N2	CTS	input	controlling signal [1)]
N3	RTS	output	controlling signal [1)]
N4	TxD	output	data signal
N5	RxD	input	data signal
N6	GND	signal ground	

[1)] Use of the signal is described in the handbook *Serial Communication of Tecomat Programmable Logic Controllers, TXV 001 06.02*. Still level of the signal corresponds with the value of logical 1.

In Fig. 9.27, five-conductor interconnection with the possibility of CTS signal detection is shown.

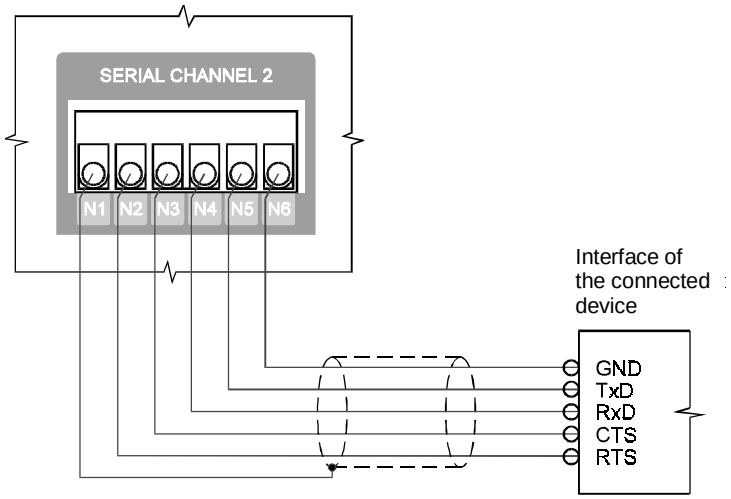


Fig. 9.27 Five-conductor interconnection of the CH2 interface RS-232 of the PLC of TC600 series

Fig. 9.28 shows three-conductor interconnection of data binding circuits. The dashed line indicates formation of the RTS-CTS loop.

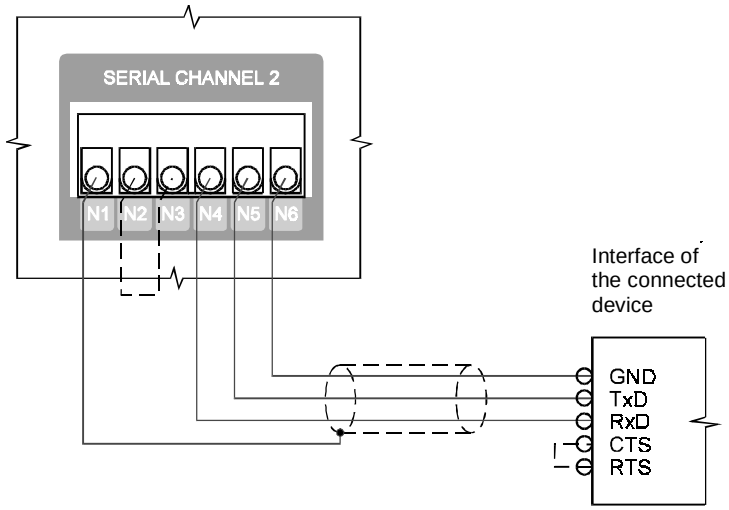


Fig. 9.28 Three-conductor interconnection of the CH2 interface RS-232 of the PLC of TC600 series

Optional CH2 RS-485 interface

Binding circuits of the interface are led out to connectors N1 to N6 of the terminal board marked as SERIAL CHANNEL 2.

Lead out of binding circuits of piggybacks MR-04, MR-09 of CH2

Connector	Signal	Signal type	Use
N1		frame	connection of the shielding
N2, N4	RxD-/TxD-	input/output	data signal
N3, N5	RxD+/TxD+	input/output	data signal
N6	GND	signal ground	

Interconnection is realized in the way described under item 9.5.9.

Optional CH2 RS-422 interface

Binding circuits of the interface are led out to connectors N1 to N6 of the terminal board marked as SERIAL CHANNEL 2.

Lead out of binding circuits of the piggyback MR-17 of CH2

Connector	Signal	Signal type	Use
N1		frame	connection of the shielding
N2	TxD-	output	data signal
N3	TxD+	output	data signal
N4	RxD-	input	data signal
N5	RxD+	input	data signal
N6	GND	signal ground	

Interconnection is realized in the way described under item 9.5.9.

9.5.11 Connection of the CH3 Interface

CH3 RS-232 interface

Binding circuits of the interface are led out to connectors P1 to P5 of the terminal board marked as OPTIONAL I/O.

Lead out of binding circuits of the piggy-back MR-15 of CH3

Lead out	Signal	Signal type	Use
P1	TxD	output	data signal
P2	RTS	output	controlling signal [1)]
P3	RxD	input	data signal
P4	CTS	input	controlling signal [1)]
P5	GND	signal ground	

[1)] Use of the signal is described in the handbook *Serial Communication of Tecomat Programmable Logic Controllers, TXV 001 06.02*. Still level of the signal corresponds with the value logical 1.

Interconnection is realized in the way described under item 9.5.10.

CH3 RS-485 interface

Binding circuits of the interface are led out to connectors P6 to P10 of the terminal board marked as OPTIONAL I/O.

Lead out of binding circuits of the piggy-back MR-14 of CH3

Connector	Signal	Signal type	Use
P6, P8	RxD+/TxD+	input/output	data signal
P7, P9	RxD-/TxD-	input/output	data signal
P10	GND	signal ground	

Interconnection is realized in the way described under item 9.5.9.

9.5.12 Connection of Interrupt Inputs

Interrupt inputs are connected identically as common binary inputs (see item 9.5.3).

9.5.13 Connection of the Type 3 Counter

Source of counted events and the controlling signal are connected between the common connector A1 (COM1) and connectors A2 (DI0) and A3 (DI1) in the way illustrated in the scheme in Fig. 9.29. In the case that the RESET input is not used, it must be serviced by connection to voltage corresponding with log. 1.

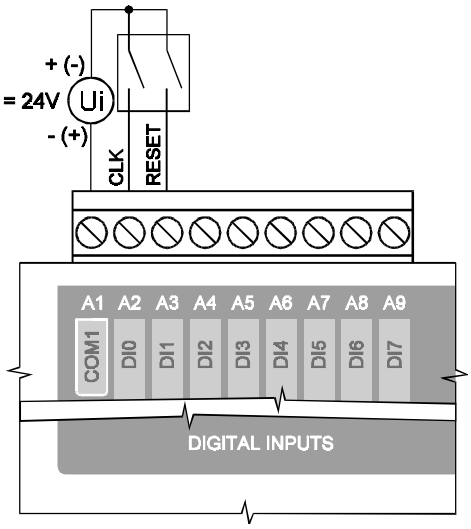
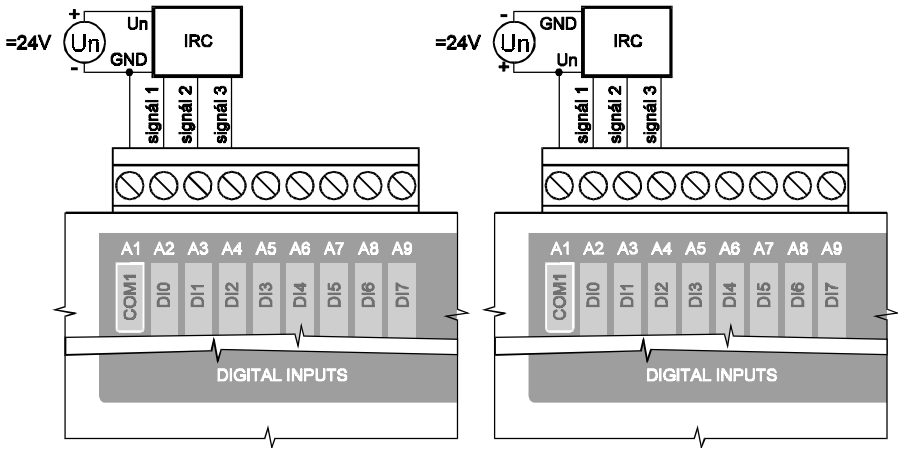


Fig. 9.29 Connection of the type 3 counter of the PLC of TC600 series

9.5.14 Incremental Encoder Connection

Incremental encoder is connected between the common connector A1 (COM1) and connectors A2 (DI0) to A4 (DI2) in the way illustrated in the scheme in Fig. 9.30.



signal 1 - direct output of trace 1
signal 2 - direct output of trace 2
signal 3 - direct output of the zero pulse

Fig. 9.30 Connection of the incremental encoder with outputs with the open PNP collector (on the left) and NPN collector (on the right) to the PLC of TC600 series

9.5.15 Connection of Inputs for Measurement of the Period and Phase Shift

Measurement inputs are connected identically as common binary inputs (see item 9.5.3).

10. Attendance

10.1 Instructions for Safe Attendance

When the power supply is on, it is not allowed to disconnect and connect supplying terminal boards neither to connect and disconnect individual conductors of the terminal boards.

When programming controlling PLC algorithms, the possibility of an error in the user program cannot be excluded the result of which may be unexpected behaviour of the controlled object the consequence of which may be origination of breakdown situation and in the extreme case also endangering of persons. In attendance to the PLC, especially in the testing stage and debugging of new user programs with the controlled object, it is unconditionally necessary to be concerned with greater carefulness.

The producer is not responsible for damages caused by improper attendance or incorrect algorithm of the user program.

10.2 Putting into Operation

When putting the PLC into operation for the first time, it is necessary to meet the following procedure:

- check correctness of the connection and voltage value of the PLC power supply
- check interconnection of the PLC protective connectors with the main protective connector of the distribution board or case
- check correctness of the connection and voltage value of the power supply of input and output circuits
- turn on the PLC power supply

10.3 PLC Initialization

After the power supply is turned on, the PLC transfers to the starting sequence. The starting sequence is used for testing of the program and technical equipment of the PLC and setting of the PLC to the defined initial state.

In the course of the starting sequence, version of the system program equipment is gradually shown on the display, for example:

4_0

PLC binary outputs are blocked in the still state in the course of the testing (the BLK signal is lighted in the field of binary outputs) and analog outputs are set to zero.

The starting sequence may be terminated by transferring to the RUN mode and displaying

G,

by transferring to the HALT mode and displaying

H,

by transferring to the SET mode (see Article 4.5) or transferring to the HALT mode with displaying of the error message

t.E, E or full error code, for example E-80-09-00-00.

10.4 Operational Modes

The PLC may operate in three basic modes.

Mode RUN

The RUN mode is a common operational mode in which values of input signals are scanned, operations given by the user program algorithm are performed, and PLC outputs are set. The PLC transfers in the RUN mode automatically after proper termination of the starting sequence. In the course of the mode, letter G is shown on the display.

Mode HALT

The HALT mode is an operational mode in which the user program is not run and the PLC is in a defined state. The PLC transfers to the HALT mode automatically when a critical error is evaluated during the starting sequence or in the course of control and after termination of the SET mode.

If the PLC transfers to the HALT mode from the starting sequence, binary outputs remain blocked in the still state, analog outputs remain set to zero and code of the error message is shown on the display.

If the PLC transfers in the HALT mode after termination of the SET mode, binary outputs remain blocked in the still state, analog outputs remain set to zero and letter H or an error message are is shown on the display. Mode HALT evoked by termination of the SET mode can be terminated either by the superior system or by turning off and on of the PLC power supply.

If the PLC transfers to the HALT mode in the course of control, binary outputs are set in the still state and blocked, analog outputs are frozen in the state in which they were in the moment of transferring to the HALT mode, and an error message is shown on the display.

For transfer to the HALT mode controlled by the user see item 10.4.1.

Mode SET

The SET mode serves for setting of communication parameters, setting of the time circuit, and control of activation of the source user program. Entrance in the mode is controlled by the attendance persons at turning on of the PLC power supply. In the course of the mode, binary outputs are blocked in the still state, and analog outputs are set to zero. After termination of the SET mode, the PLC transfers automatically to the HALT mode. Detailed description of setting of the PLC parameters is given in Article 4.5.

10.4.1 Change of Operational Modes

Transfer between RUN and HALT modes controlled by the attendance persons is possible only using the superior system equipped with an integrated development environment for programming of the Tecomat PLC's or with a monitoring and controlling program. Transfer between the modes has practical foundation only in the phase of debugging of the user program. In general, it can be said that transfer between the modes if a device is connected, especially modification of the PLC activity at transfer between the modes, requires perfect knowledge of the controlled object as well as of the PLC, and careful consideration of possible consequences.

When changing the PLC operational modes, some activities are performed on the standard basis, and some can be performed optionally. In the case that the change of the PLC mode is done using the PLC development environment, optional activities at changing of the mode are a part of the development environment menus.

10.4.2 Activities Performed at Changing of the PLC Mode on the Standard Basis

Transfer from the HALT to RUN mode

In transfer from the HALT to RUN mode, the following is performed:

- test of the user program integrity
- check of software configuration given in the user program (see item 10.5.2)
- running of the user program solving

Transfer from the RUN to HALT mode

In transfer from the RUN to HALT mode, the following is performed:

- stopping of the user program solving
- setting of outputs in a defined state

If a critical error occurs in the course of activities performed at transfer between the modes, the PLC sets the HALT mode, shows on the display the error code, and expects removal of the error cause.

Do not in any case replace stopping of control using the HALT mode by function of the button CENTRAL STOP.

10.4.3 Optionally Performed Activities at Change of the PLC Mode

Options at transfer from HALT to RUN

At transfer from the HALT mode to RUN, it is possible to optionally perform the following:

- resetting of the PLC error
- warm or cold reboot
- blocking of outputs at solving of the user program

Options at transfer from RUN to HALT

At transfer from the RUN mode to HALT, it is possible to optionally perform the following:

- resetting of the PLC error
- setting of the PLC outputs to zero

At resetting of the PLC error, the whole PLC error stack is reset.

The request for blocking of the PLC outputs causes the program to be solved with disconnected binary outputs. Blocking of the outputs is indicated by the BLK LED diode in the field of binary outputs.

At setting of the outputs to zero, all images of the PLC binary outputs are set to zero.

10.4.4 Restarts of the User Program

Restart means such a PLC activity, the purpose of which is prepare the PLC for solving of the user program. Under normal circumstances, restart is performed after turning on of the power supply, and at every change of the user program.

The systems distinguish two types of restart, warm and cold. Warm restart allows for retaining of the values in the remanent part of the scratchpad. Cold restart is always performed with full memory initialization.

Activities performed during restart

During restart, the following is performed:

- test of integrity of the user program
- resetting of the whole PLC scratchpad
- resetting of the remanent zone (only at cold restart)
- setting of the remanent zone (only warm restart)
- initialization of system registers S
- initialization and checking of PLC inputs and outputs

Running of the program without restart

When the user program is run without a restart, only test of integrity of the user program is performed and checking of the PLC inputs and outputs.

Restarts after turning on

After being turned on, the PLC performs the restart type chosen by the user. If damage of data found in the remanent zone of the scratchpad memory is evaluated, PLC performs cold restart without regard to the chosen restart type.

User processes at restart

Depending on the performed restart, the planning unit of user processes P operates as well. If you have performed warm restart at transfer from the HALT to RUN mode, after transferring to the RUN mode the user process P62 is solved first (if programmed). At cold restart, after transferring to the RUN mode the user process P63 is solved first (if programmed). If only one of the processes P62, P63 is programmed, then this process is performed in the case of warm as well as cold restart. If the process P62 neither P63 is programmed, then process P0 is solved first after transfer to the RUN mode.

Change of the program during PLC operation

Programming of the xPRO environment allows for change of the program during PLC operation. Here it is necessary to keep in mind that during

recording of the new program, solving of the program is stopped without blocking of outputs. This state may last even several seconds!

10.5 Programming and Debugging of the PLC Program

PLC programming

Programming of control algorithms and testing of correctness of the written programs for TECOMAT PLC's is performed using computers of the PC standard. For connection with the PLC, the serial channel of these computers is used.

Diskette with examples and the xPRO development environment in the version xPRO Lite and xPROm is delivered with every PLC.

Examples of PLC programs contain instructions for attendance of various PLC units.

xPRO development environment

The xPRO integrated development environment is available in the following versions:

xPRO - full version with the hw key for professional work
xPRO Lite - freely distributable version without the hw key
xPROm - freely distributable version intended for checking of the technology operation with exclusion of the possibility of interventions in the PLC user program

The xPRO development environment has the following properties:

- integrated environment Turbo Vision including the editor
- possibility to work with several files at the same time, every one of them having its own window
- compiler into the machine code of processors of all series
- symbolic names of labels and operands
- automatic assignment of variables
- generation of the symbols table and cross references
- creation of macro-instructions
- backward compilation of the program
- built-in simulator of the TECOMAT PLC
- full use of the PLC debugging means
- automatic generation of configuration according to the connected PLC
- contact plan (relay line schemes) with partial lighting of connection paths in the debugging mode
- integrated sensitive help system containing the whole programmer's handbook
- control using the mouse or the keyboard with the possibility to use both the program menus (pull down menus) as well as the direct selection realized by pressing of a key combination (hot keys)

10.5.1 Configuration Constants in the User Program

Configuration of constants for setting of services provided during the PLC operation

Configuration constants are automatically generated during compilation of the user program, and they form its non-separable part. They carry information on the required PLC mode and its use. Constants can be set using menus of the xPRO integrated compiler environment before the compilation itself.

Configuration constants contain the following services:

- type of restart after turning on of the PLC power supply
  This determines whether after turning on of the power supply, warm or cold restart will be performed (see item 10.4.4). Cold restart is the default setting.
- time of issuing the first warning of threat of exceeding of the maximum allowed cycle time
  If the cycle of processing the user program lasts longer than the time defined by this constant, PLC system services set the bit S2.7 as a flag that in processing of the program, the set time has been exceeded in this cycle, and at the same time the soft error code is set in the system register S34 and S48 to S51. Default set value is 150 ms.
- time of guarding the maximum allowed cycle time
  If the cycle of processing of the user program lasts longer than the maximum allowed cycle time, PLC announces critical error of exceeding the cycle time, blocks the outputs and interrupts cycling running of the user program. This constant defines the longest possible time during which the controlled object may remain without an action intervention. The default set value is 250 ms, the recommended maximum value is 500 ms.
- determining of the extent of backup of the user program in EEPROM
  Defines whether the whole user program is backed including tables T or whether the user program is backed without the tables T and tables T remain in the original version in backed RAM (suitable in cases of modification of the tables by the user program). Backing of the whole user program is the default setting.
- number of backed registers R (remanent zone)
  Setting of the number of backed registers R values of which will be saved in the case of the PLC power supply failure, ensured by the checking character, and retrieved in the case of warm restart of the PLC. Registers are saved starting from register R0, state of the registers after the last fully terminated cycle of solving of the user program is backed. Default set value is 0.

10.5.2 Software Configuration

Software and hardware configuration

Software (sw) configuration of inputs and outputs describes the PLC set, and forms a non-separable part of the user program. Before running of solving of the user program, this description is compared with reality found out during the PLC starting sequence (the so called hardware configuration). It allows for perfect checking of readiness of the whole PLC for the control before running the program. At the same time, the user gains the possibility to practically arbitrarily assign placement of images of inputs and outputs in zones X, Y, R, and gradually activate inputs and outputs at debugging of the program without the necessity of physical disconnection or connection of the terminal boards.

In the xPRO program, sw configuration is entered using the directive *#unit*. Structure of the directive is identical with other Tecomat PLC directives. Some parameters intended for description of more extensive system, have the character of a constant in the TC600 series.

General structure of the directive is as follows:

```
#unit MODUL, ADR, TYP, POC_IN, POC_OUT, Z_IN, Z_OUT, AKT,
      INITAB
```

`MODUL` - always 0 for the TC600 series

`ADR` - always 0 for BM binary and analog inputs and outputs
- always 1 for binary inputs and outputs and analog inputs of the first EM/2
- always 2 for binary inputs and outputs and analog inputs of the second EM/2
- always 2 for EM binary inputs and outputs and analog inputs
- always 2 for the CH2 serial channel
- always 3 for the CH3 serial channel

`TYP` - type of inputs or outputs

`$10` - serial channel CH2 or CH3

Parameters `MODUL, ADR, TYP` of serial channel `2 (3)` can be entered together in the symbolic way `CH2 (CH3)`

`$80` - EM/2 binary inputs or outputs (TC631, TC632)

`$90` - EM/2 binary inputs or outputs (TC633)

`$A0` - EM, BM binary inputs or outputs

Parameter `TYP` of binary inputs or outputs can be entered for the BM and EM symbolically as `Digit_600, for` EM/2 `Digit_63x` (TC631, TC632) and `Digit_633` (TC633)

`$D0` - analog inputs or outputs

Parameter `TYP` of analog inputs or outputs can be entered form BM, EM and EM/2 symbolically as `Analog_600_`

`POC_IN` - number of input bytes

`POC_OUT` - number of output bytes

`Z_IN` - placement of the first input byte in the scratchpad

`Z_OUT` - placement of the first output byte in the scratchpad

The parameter is entered absolutely, for example `Y0, R128` ..., or symbolically

`AKT` - activation of servicing of inputs or outputs

Parameter is entered symbolically

- `X_On` - activation of servicing of inputs
- `X_Off` - servicing of inputs is not activated
- `Y_On` - activation of servicing of outputs
- `Y_Off` - servicing of outputs is not activated
- `On` - simultaneous activation of servicing of inputs as well as outputs
- `Off` - servicing of inputs neither outputs is activated

`INITAB` - address of the table containing the initialization data
Parameter is entered symbolically, for example `IniCH2,` or absolutely, for example `T0` (names used in the following examples of declarations are not mandatory).
Entering of the parameter for CH2, CH3, analog inputs and some special functions (see further) is mandatory. The parameter is not entered for binary inputs and outputs.

Declaration of special functions

Another possibility of the sw configuration is declaration of the PLC special functions. Special function use standard-fitted PLC inputs and outputs, however their servicing requires more complicated shell algorithms or complementation of the basic technical equipment of the input and output unit. These servicing algorithms are realized by the system, thus servicing by the user program remains simple.

Automatic generation of the sw configuration

The xPRO program contains the function for automatic generation of sw configuration according to the connected PLC type and its further editing. This enables the user to have the sw configuration created exactly according the real technical equipment or create a basis for the user's own declaration of inputs, outputs, and functions of the PLC set.

Solving of the user program with disconnected inputs and outputs

If no sw configuration is entered in the user program, the program will be solved only above the PLC scratchpad memory and the PLC inputs and outputs will not be serviced. Binary outputs will remain blocked in this case and analog outputs will remain set to zero.

10.5.3 Servicing of Binary Inputs

Declaration of BM binary inputs

BM binary inputs are assigned to the scratchpad memory together with binary outputs by the directive `#unit` with general structure according to 10.5.2.

Example of declaration for TC601 BM

```
#unit 0, 0, Digit_600, 2, 1, X0, Y0, On
                    ; binary inputs and transistor outputs
```

Example of declaration for TC602 BM

```
#unit 0, 0, Digit_600, 3, 2, X0, Y0, On
                    ; binary inputs and transistor outputs
```

Example of declaration for TC603 BM

```
#unit 0, 0, Digit_600, 2, 1, X0, Y0, On
              ; binary inputs and transistor and relay outputs
```

Example of declaration for BM of TC604, TC605, TC606

```
#unit 0, 0, Digit_600, 2, 2, X0, Y0, On
                    ; binary inputs and relay outputs
```

Example of declaration for TC607

```
#unit 0, 0, Digit_600, 3, 3, X0, Y0, On
              ; binary inputs and transistor outputs
```

Declaration of EM binary inputs

EM binary inputs are assigned to the scratchpad memory together with binary outputs by the directive `#unit` with general structure according to 10.5.2.

Example of declaration for TC621 EM

```
#unit 0, 2, Digit_600, 2, 1, Xn, Yn, On
              ; binary inputs and transistor outputs
```

Example of declaration for TC622 EM

```
#unit 0, 2, Digit_600, 3, 2, Xn, Yn, On
              ; binary inputs and transistor outputs
```

Example of declaration for TC623 EM

```
#unit 0, 2, Digit_600, 2, 1, Xn, Yn, On
              ; binary inputs and transistor and relay outputs
```

Example of declaration for EM of TC624, TC625, TC626

```
#unit 0, 2, Digit_600, 2, 2, Xn, Yn, On
              ; binary inputs and relay outputs
```

Placement of images of inputs (parameter Xn) and outputs (parameter Yn) depends on the type and fitting of the BM or possibly on the type of EM/2 of the PLC set.

Declaration of EM/2 binary inputs

EM/2 binary inputs are assigned to the scratchpad memory together with binary outputs (TC631, TC632) or individually (TC633) by the directive `#unit` with general structure according to 10.5.2.

Example of declaration for TC631 EM/2

```
#unit 0, ADR, Digit_63x, 1, 1, Xn, Yn, On
                    ; binary inputs and transistor outputs
```

Example of declaration for TC632 EM/2

```
#unit 0, ADR, Digit_63x, 1, 1, Xn, Yn, On
                    ; binary inputs and relay outputs
```

Example of declaration for TC633 EM/2

```
#unit 0, ADR, Digit_633, 2, 0, Xn, 0, On
                    ; binary inputs
```

The module address (parameter ADR) depends on placement of the module towards the BM. Address 1 is assigned to the first EM/2, address 2 is assigned to the second EM/2. Placement of images of inputs (parameter Xn) and outputs (parameter Yn) depends on the type and fitting of the BM, or possibly on the type of the first EM/2 of the PLC set. In automatic generation of the sw configuration, images of inputs and outputs of BM, EM/2 and EM form a continuous series.

Servicing of binary inputs

Binary inputs of BM, EM and EM/2 occupy in the inputs image in the scratchpad 1 to 3 bytes depending on the module type (parameter of the directive `#unit POC_IN = 1, 2 or 3`). State of signals at the PLC inputs is overwritten in the cycle loop in the scratchpad zone with the initial address defined by the parameter `Z_IN` of directive `#unit`.

Structure of binary inputs zone

Zone of binary inputs in the scratchpad has the following structure:

bit	.7	.6	.5	.4	.3	.2	.1	.0	
	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	Z_IN
	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	Z_IN+1
					DI19	DI18	DI17	DI16	Z_IN+2

Besides the way given above, binary inputs are accessible by direct reading of instructions LD with the operand U and the physical input address. For structure of the physical address see item 10.5.12.

10.5.4 Servicing of Binary Outputs

Declaration of binary outputs

Binary outputs are assigned to the scratchpad memory together with binary inputs by the directive `#unit` with general structure according to 10.5.2. For examples of declaration see 10.5.3.

Servicing of binary outputs

Binary outputs of BM, EM and EM/2 occupy in the outputs image in the scratchpad 1, 2 or 3 bytes depending on the module type (parameter of the directive `#unit POC_OUT = 1, 2 or 3`). Setting of the outputs is done in the cycle loop according to the state of the outputs image with the initial address defined by the parameter `Z_OUT` of directive `#unit`.

Structure of binary outputs zone

Zone of binary outputs in the scratchpad has the following structure:

bit	.7	.6	.5	.4	.3	.2	.1	.0	
	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	Z_OUT
	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	Z_OUT+1
					DO19	DO18	DO17	DO16	Z_OUT+2

Besides the way of outputs control given above, binary outputs are accessible by direct writing of instructions WR with the operand U and the physical output address. For structure of the physical address see item 10.5.12.

Checking of overload of binary outputs

PLC's of the TC600 series allows for program-checking of outputs overload. This state is signalled at bit S35.1:

S35.1 = 0 - outputs are in correct state
S35.1 = 1 - overload of outputs

When S35.1 = 1, the soft PLC error is also evoked with the code 40 00 50 A0, signalled in S34 and S48 to S51.

10.5.5 Servicing of Analog Inputs

Declaration of analog inputs

Analog inputs of BM, EM and EM/2 are assigned to the scratchpad memory by the directive `#unit` with general structure according to 10.5.2. Parameter `INITAB` of the directive is mandatory. In the case that the BM is fitted with the piggyback OT-13 or OT-14, analog inputs are declared together with the BM analog outputs.

Example of declaration for BM of TC605 and TC606

```
#unit 0, 0, Analog_600_, 8, 0, X2, 0, On, IniAI
                          ; analog inputs
```

Example of declaration for EM of TC625 and TC626

```
#unit 0, 2, Analog_600_, 8, 0, X2, 0, On, IniAI
                          ; analog inputs
```

Placement of image of inputs (parameter Xn) or possibly of outputs (parameter Yn) depends on the type and fitting of the BM, or possibly on the type of EM/2 of the PLC set.

Example of declaration forTC634 EM/2

```
#unit 0, ADR, Analog_600_, 16, 0, Xn, X_On, Ini634
                          ; analog inputs
```

Module address (parameter ADR) depends on placement of the module towards the BM. Address 1 is assigned to the first EM/2, address 2 is assigned to the second EM/2. Placement of the image of inputs (parameter Xn) depends on the type and fitting of the BM, or possibly of the type of the first EM/2 of the PLC set. In automatic generation of sw configuration, images of inputs and outputs of BM, EM/2 and EM form a continuous series.

Servicing of analog inputs of TC605, TC606 and TC625, TC626

Analog inputs of TC605 and TC606 BM, and of TC625 and TC626 EM, occupy 8 bytes in the inputs image in the scratchpad (parameter of the directive `#unit POC_IN = 8`). Binary representation of the inputs state is overwritten in the cycle loop into the scratchpad zone with the initial address defined by the parameter `Z_IN` of directive `#unit`.

Structure of analog inputs zone of TC605, TC606 and TC625, TC626

Zone of analog inputs in the scratchpad has the following structure:

AI0	.7	.6	.5	.4	.3	.2	.1	.0	Z_IN
					.11	.10	.9	.8	Z_IN+1
AI1	.7	.6	.5	.4	.3	.2	.1	.0	Z_IN+2
					.11	.10	.9	.8	Z_IN+3
	.								
	.								
AI3	.7	.6	.5	.4	.3	.2	.1	.0	Z_IN+6
					.11	.10	.9	.8	Z_IN+7

Setting of analog inputs range of TC605, TC606 and TC625, TC626

Besides the way of control given above, analog inputs are accessible by direct reading of instructions LD with the operand U and physical input address. For structure of the physical address see item 10.5.12.

Range of analog inputs is set in the initialization table with the name defined by the parameter `INITAB` of directive `#unit`. The table contains 1 byte with the following meaning:

.7	.6	.5	.4	.3	.2	.1	.0
				range AI3	range AI2	range AI1	range AI0

value of the appropriate bit 0 = voltage range 0 to +10 V
value of the appropriate bit 1 = voltage range 0 to +2 V
For the current range of 0 to 20 mA, the appropriate bit is set to value 1.

Example of analog inputs initialization table o TC605, TC606 and TC625, TC626

```
#table byte IniAI = %00000011
                          ;range of inputs AI0, AI1 0 to 2 V
                          ;range of inputs AI2, AI3 0 to 10 V
```

Servicing of TC634 analog inputs

TC634 analog inputs occupy 16 bytes in the inputs image in the scratchpad (parameter of the directive `#unit POC_IN = 16`). Binary representation of the inputs state is overwritten in the cycle loop into the scratchpad zone with the initial address defined by the parameter `Z_IN` of directive `#unit`.

Structure of TC634 analog inputs zone

Zone of analog inputs in the scratchpad has the following structure:

AI0	.7	.6	.5	.4	.3	.2	.1	.0	Z_IN
	.15	.14	.13	.12	.11	.10	.9	.8	Z_IN+1
AI1	.7	.6	.5	.4	.3	.2	.1	.0	Z_IN+2
	.15	.14	.13	.12	.11	.10	.9	.8	Z_IN+3
					.				
					.				
AI7	.7	.6	.5	.4	.3	.2	.1	.0	Z_IN+14
	.15	.14	.13	.12	.11	.10	.9	.8	Z_IN+15

TC634 analog inputs are not accessible by direct reading of instruction LD with the operand U and the physical input address.

Setting of type of inputs, measurement ranges and formats of input data of TC634

Type of inputs, the measurement range and format of input data of TC634 analog inputs is set in the initialization table with the name defined by the parameter `INITAB` of directive `#unit`. The table contains 8 items of the type word with the following meaning:

Structure of the TC634 initialization table

```
#table word Ini634 = CONT 0,     ;setting of input AI0
                     CONT 1,     ;setting of input AI1
                     CONT 2,     ;setting of input AI2
                     CONT 3,     ;setting of input AI3
                     CONT 4,     ;setting of input AI4
                     CONT 5,     ;setting of input AI5
                     CONT 6,     ;setting of input AI6
                     CONT 7      ;setting of input AI7
```

Structure of the TC634 control word CONT

The CONT control word has the following structure:

.15	.14	.13	.12	.11	.10	.9	.8	.7	.6	.5	.4	.3	.2	.1	.0
AK	-	-	-	-	-	V1	V0	SN3	SN2	SN1	SN0	TP3	TP2	TP1	TP0

TP0-TP3	selection of scanner type or range
SN0-SN3	selection of input type
V0-V1	format of input data
AK	channel activation 0 = channel off 1 = channel on

Valid values of the TC634 control word

The following table gives allowed values of the CONT control word with the corresponding selections:

CONT	Input type	Scanner/range type	Format of input data [1)]
$8020	Resistance temperature scanners	Pt100, W100 = 1.385	0 to 65535
$8120		-200 to +850 °C	-2000 to +8500 [0.1°C]
$8022		Pt100, W100 = 1.391	0 to 65535
$8122		-200 to +850 °C	-2000 to +8500 [0.1°C]
$8027		Ni1000, W100 = 1.617	0 to 65535
$8127		-60 to +200 °C	-600 to +2000 [0.1°C]
$8029		Ni1000, W100 = 1.500	0 to 65535
$8129		-60 to +200 °C	-600 to +2000 [0.1°C]
$8030	Resistance scanners	0 to 630 Ω	0 to 65535
$8130			0 to 6300 [0.1 Ω]
$8230			0 to 10000
$8032		0 to 2520 Ω	0 to 65535
$8132			0 to 25200 [0.1 Ω]
$8232			0 to 10000
$8040	Current	0 to 20 mA	0 to 65535
$8140			0 to 20000 [μA]
$8240			0 to 10000
$8042		4 to 20 mA	0 to 65535
$8142			40000 to 20000 [μA]
$8242			0 to 10000
$8080	Voltage	0 to 10 V	0 to 65535
$8180			0 to 10000 [1 mV]
$8280			0 to 10000
$8082		0 to 2 V	0 to 65535
$8182			0 to 20000 [0.1 mV]
$8282			0 to 10000

[1)] For details see item 5.1.5

The following example gives declaration of the TC634 module connected according to Figs. 9.21 a 9.22.

Example of TC634 declaration

```
#table word Ini634 = $8140, ;AI0 - 0 to 20mA/µA
                     $8142, ;AI1 - 4 to 20mA/µA
                     $8180, ;AI2 - 0 to 10V/mV
                     $8182, ;AI3 - 0 to 2V/0,1mV
                     $8120, ;AI4 - Pt100, W100 = 1.385/0,1°C
                     $8122, ;AI5 - Pt100, W100 = 1.391/0,1°C
                     $8127, ;AI6 - Ni1000, W100 = 1.617/0,1°C
                     $8129  ;AI7 - Ni1000, W100 = 1.500/0,1°C

#unit 0, 1, Analog_600_, 16, 0, R0, X_On, Ini634
                           ; TC634 in position 1. EM
                           ; data from R0
```

10.5.6 Servicing of Analog Outputs

Declaration of optional analog outputs

In the case of fitting the optional piggyback OT-13 or OT-14, the sw configuration of BM standard-fitted inputs and outputs is complemented in the way which depends on the BM type.

Declaration of the piggyback OT-13 and OT-14 in BM of TC601 to TC604

In BM of TC601 to TC604, the sw configuration is complemented by the new directive `#unit` for the piggyback OT-13 or OT-14. Example of the directive:

```
#unit 0, 0, Analog_600_, 0, 4, 0, Yn, On
                          ; analog outputs of OT-13
#unit 0, 0, Analog_600_, 0, 8, 0, Yn, On
                          ; analog outputs of OT-14
```

Placement of image of outputs (parameter Yn) depends on the BM type (is linked to image of binary outputs).

Declaration of the piggyback OT-13 and OT-14 in BM of TC605, TC606

In BM of TC605 and TC606, the directive `#unit` of analog inputs and outputs is complemented by parameters for the piggyback OT-13 or OT-14. Examples of the extended directive:

```
#unit 0, 0, Analog_600_, 8, 4, X2, Yn, On, IniAI
                          ; analog inputs of BM
                          ; and analog outputs of OT-13
#unit 0, 0, Analog_600_, 8, 8, X2, Yn, On, IniAI
                          ; analog inputs of BM
                          ; and analog outputs of OT-14
```

Placement of image of outputs (parameter Yn) depends on the BM type (is linked to the image of binary outputs).

Servicing of analog outputs

BM analog outputs occupy 4 or 8 bytes in the image of outputs in the scratchpad, depending on the type of the fitted piggyback (parameter of the directive `#unit POC_OUT = 4 or 8`). Setting of the outputs according to the binary representation of levels written in images of outputs is done in the cycle loop. Initial address of the zone in the scratchpad is defined by the parameter `Z_OUT` of directive `#unit`

Structure of analog outputs zone

Zone of images of analog outputs in the scratchpad has the following structure:

AO0	.7	.6	.5	.4	.3	.2	.1	.0	Z_0UT
AO1	.7	.6	.5	.4	.3	.2	.1	.0	Z_OUT+1
					.				
					.				
AO7	.7	.6	.5	.4	.3	.2	.1	.0	Z_OUT+7

Besides the way of outputs control given above, analog outputs are accessible by direct writing of instructions WR with the operand U and the physical output address. For structure of the physical address see item 10.5.12.

10.5.7 Servicing of Serial Channels

Declaration of serial channels CH1, CH2, CH3

Declaration of CH1 is not performed.

CH2 is assigned to the scratchpad memory by the directive `#unit` with general structure according to 10.5.2.

CH3 is declared in the case that the optional piggyback MR-14 or MR-15 is fitted, and in the same way as CH2.

Automatically generated sw configuration contains the directive `#unit` for CH2 and CH3 only after previous writing of the directive by the user.

Example of CH2 and CH3 declaration for BM of TC601 to TC606

```
#unit 0, 2, _CHx, 255, 255, R0, R255, On, IniCH2
                          ; serial channel CH2

#unit 0, 3, _CHx, 255, 255, R510, R764, On, IniCH3
                          ; serial channel CH3
```

Servicing of CH1, CH2, CH3 depends on the set mode. CH1 has fixed-set mode PC, channels CH2 and CH3 have selectable modes (see Article 4.4 and 4.5). Detailed description of the modes including the servicing table is given in the handbook *Serial Communication of Tecomat Programmable Logic Controllers, TXV 001 06.02*.

10.5.8 Servicing of Interrupt Inputs

Declaration of interrupt inputs

Declaration of interrupt inputs is done by the directive `#unit` with general structure according to item 10.5.2. Parameter `INITAB` of the directive is mandatory. The initialization table serves for definition of edges of signals which evoke the interrupt request (IRQ).

Structure of the initialization table

```
#table byte IniTable = item 1,   ;DI0 control
                       item 2,   ;DI1 control
                       item 3,   ;DI2 control
                       item 4    ;DI3 control
```

Items 1 to 4 may have the following values:
0 - without IRQ
1 - IRQ allowed from the ascending signal edge
2 - IRQ allowed from the descending signal edge
3 - IRQ allowed from both signal edges

Declaration example

```
#def NO   0  ;without IRQ
#def UP   1  ;IRQ from the ascending signal edge
#def DOWN 2  ;IRQ from the descending signal edge
#def ALL  3  ;IRQ from both signal edges
;
#table byte IniIRQ = all, ;IRQ from both edges of input 0
                     up, ;IRQ from ascending edge of input 1
                   down, ;IRQ from descending edge of input2
                     no  ;without IRQ from input 3
;
#unit 0, 0, IntIn_600_, Xn, Yn, On, IniIRQ
;
```

Parameter `TYP, POC_IN, POC_OUT` of the directive `#unit` is input symbolically as `IntIn_600_` or numerically `$20, 1, 1`. Placement of the state and control word (parameters `Xn, Yn`) depends on the BM type (on occupation of the scratchpad by images of inputs and outputs).

Servicing of interrupt inputs

Interrupt inputs occupy 1 byte in the scratchpad in the image of inputs (state word) and 1 byte in the image of outputs (control word).

State word

The STAT state word serves for distinguishing of the interrupt source. Flags of the interrupt in the state word are set before running of the P42 interrupt process. The state word placed in the scratchpad at the address defined by parameter `Z_IN` of directive `#unit` has the following structure:

-	-	-	-	STAT .3	STAT .2	STAT .1	STAT .0	Z_IN

STAT.0 = 1 - interrupt from input DI0
STAT.1 = 1 - interrupt from input DI1
STAT.2 = 1 - interrupt from input DI2
STAT.3 = 1 - interrupt from input DI3

Control word

The CONT control word serves for allowing or prohibiting an interrupt from individual inputs in the course of the program execution. It is accepted by the system after it is written to the scratchpad. The control word placed in the scratchpad at the address defined by parameter `Z_OUT` of directive `#unit` has the following structure:

-	-	-	-	CONT .3	CONT .2	CONT .1	CONT .0	Z_OUT

CONT.0 - interrupt allowed from input DI0
CONT.1 - interrupt allowed from input DI1
CONT.2 - interrupt allowed from input DI2
CONT.3 - interrupt allowed from input DI3
0 = interrupt prohibited
1 = interrupt allowed

PLC response time

PLC response time is the sum of all times with which processing of the interrupt is loaded since the rise of the interrupt request at the PLC input to closing of the output closing element. Response time is affected not only by the PLC properties, but also by the way of processing in the user program.

For better clarity, the following description contains also comparable parameters and the time diagram of processing of the input signal of standard binary inputs.

Definition of times

t_{min} - minimum width of the input pulse (minimum lasting time of one level of the input signal)
- min. 30 μs for interrupt inputs
- for standard binary inputs, at the minimum the lasting time of the program cycle

t_{IH}, t_{IL} - input delays
Signal delay at passing through the input filter.
- max. 5 μs for interrupt inputs
- typically 4 ms for standard binary inputs

t_{VP} - time of serving of the interrupt
Time from the IRQ evaluation to running of the P42 process. Most significant part of t_{VP} is formed by the time necessary to the possible finishing of the cycle loop (max. 4 ms) and time necessary to finish user program instructions being processed at the moment. In the case of some special instructions (for example PID) or user instructions (for example TER_ID05), time for the instruction execution may reach up to 10 ms.
- max. 10 ms if servicing according to Figs. 10.1 and 10.2
- not applied if servicing according to Fig. 10.3

t_{P42} - lasting time of the P42 process
- max. 5 ms if servicing according to Figs. 10.1 and 10.2
- not applied if servicing according to Fig. 10.3

t_{OC} - lasting time of the cycle loop
Time between two user program cycles following one after another. Lasting time of the cycle loop depends on the PLC set configuration.
- max. 4 ms for the TC600 series

t_C - - cycle lasting time
Lasting time of the user program cycle depends on the task extent and structure of the user program.
- not applied if servicing according to Figs. 10.1 and 10.2
- max. 2550 ms if servicing according to Fig. 10.3

t_{KC} - time until the cycle end
Time until the cycle end expresses situation which arrives at synchronization of the program response with the user program cycle
- not applied if servicing according to Fig. 10.1
- max. $t_C - t_{P42}$ if servicing according to Fig. 10.2
- max. t_C if servicing according to Fig. 10.3

t_{OH}, t_{OL} - output delay
Closing time or opening time of the output switch
- typ. 4 ms for relay outputs
- max. 400 μs for transistor outputs

t_{OP} - time of the program response (see further text)

t_{OA} - time of the programmable controller response (see further text)

Programmable controller response asynchronous to the program cycle

Time diagram in Fig. 10.1 illustrates the shortest possible response time of the programmable controller t_{OA} to change of signal at the interrupt input. In the P42 process, identification of the interrupt source is performed and servicing of the interrupt by writing to the output physical address (see item 10.5.12). Allowing of the interrupt from the ascending signal edge is assumed. Response time of the programmable controller is the sum of the following times:

$$t_{OA} = t_{IH}\ (t_{IL}) + t_{VP} + t_{P42} + t_{OH}\ (t_{OL})$$

It is apparent from the times definition that the user may affect the programmable controller response by the program structure and by selection of the output switch type. For example, if the user instruction is placed as the first or last instruction in the P0 process, in time t_{VP} the sum of times t_{OC} a t_{USI} may be applied. Exceeding of the allowed time of the interrupt process ($t_{P42} > 5$ ms) is evaluated by the diagnostic system as a serious error of the user program (see Chapter 11).

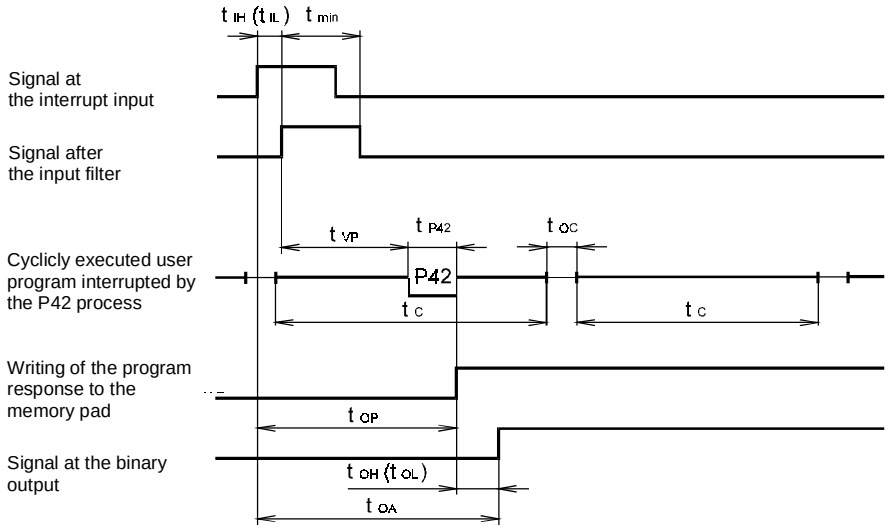


Fig. 10.1 Response time of the programmable controller to change of the signal at the interrupt input at processing of the response in the P42 process and writing to the output physical address

Response of the programmable controller synchronized with the program cycle

Time diagram in Fig. 10.2 gives prolongation of the response time of the programmable controller to change of the signal at the interrupt input at synchronization of the response with the user program cycle. In the P42 process, identification of the interrupt source is performed and servicing of the interrupt by writing to the scratchpad. Response time of the programmable controller is in this case the following sum of times:

$$t_{OA} = t_{IH}\,(t_{IL}) + t_{VP} + t_{P42} + t_{KC} + t_{OC} + t_{OH}\,(t_{OL})$$

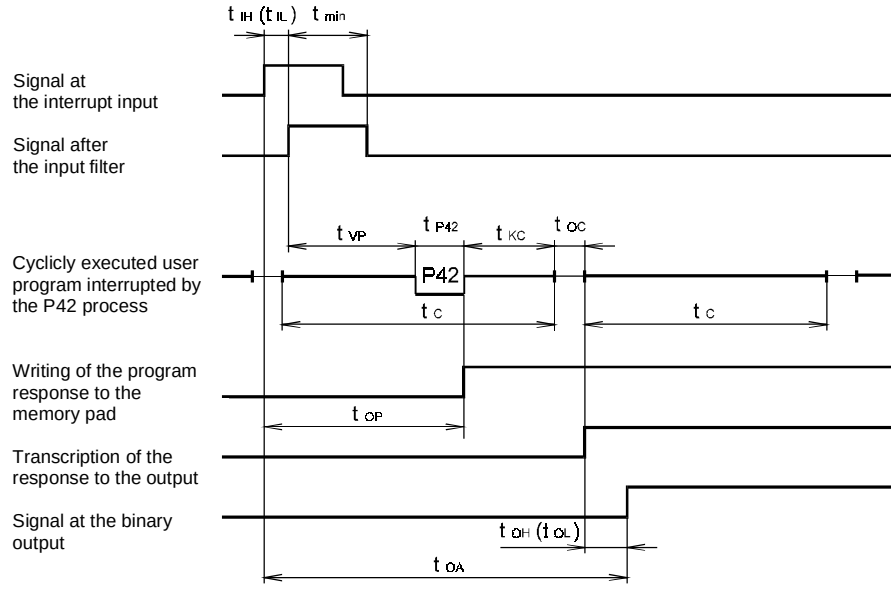


Fig. 10.2 Response time of the programmable controller to change of the signal at the interrupt input at processing of the response in the P42 process and writing to the scratchpad

Response of the programmable controller at processing of the standard binary input signal

Time diagram in Fig. 10.3 illustrates prolongation of the response time of the programmable controller to change of the signal when standard binary inputs are used (interrupt inputs in the basic mode). Response time of the programmable controller is in this case the following sum of times:

$$t_{OA} = t_{IH}\,(t_{IL}) + t_{KC} + 2t_{OC} + t_{C} + t_{OH}\,(t_{OL})$$

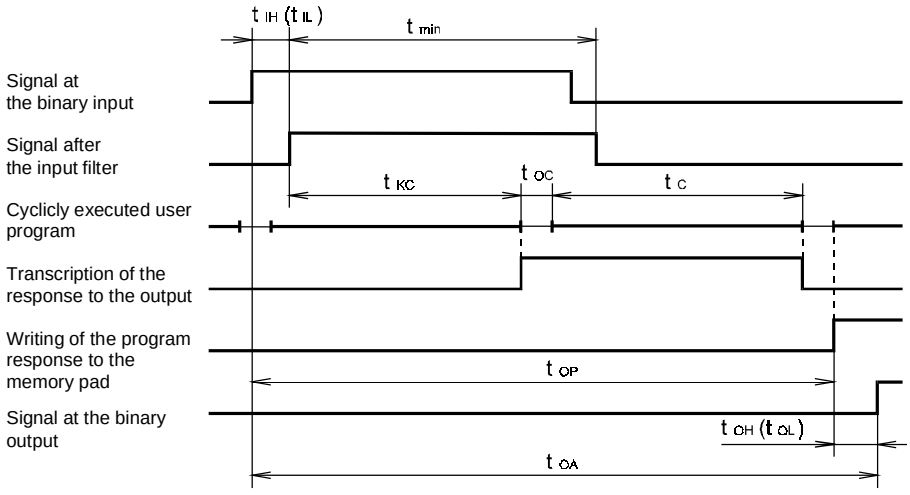


Fig. 10.3 Response time of the programmable controller to change of the signal at the standard binary input

Interrupt period

To determine the IRQ period, that it, the interval between two IRQ's from the signal at one interrupt input, it is necessary to realize that the IRQ from signals at individual interrupt inputs are asynchronous towards the program cycle, and at the same time they may be asynchronous towards one another. If the IRQ is not to be lost, it must hold that:

$$T_{IRQ} \geq \sum t_{OP\ IRQ}$$

T_{IRQ} - interrupt period
$t_{OP\ IRQ}$ - maximum response time of the program to the allowed IRQ from one edge of one signal

Meeting of this condition is illustrated in Fig. 10.4. Allowing of interrupt from the ascending as well as descending edge of the signal at DI0 is assumed, and of the ascending edge of the signal at input DI1 and descending edge of the signal at inputs DI2 and DI3.

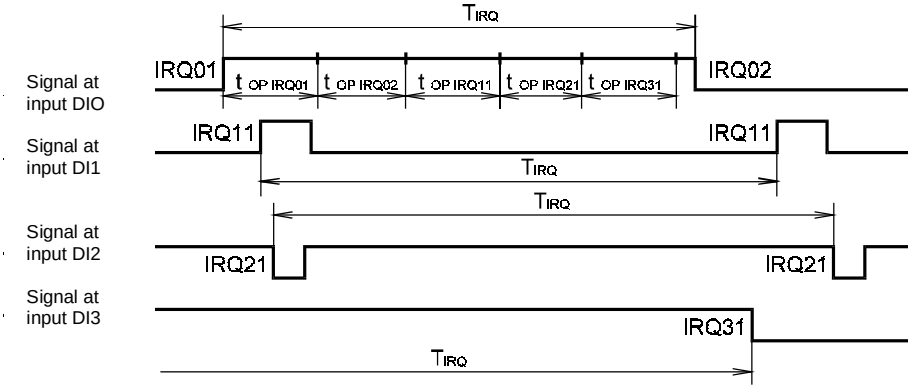


Fig. 10.4 Relation among the interrupt period, number of allowed interrupts, and response time of the program to individual interrupts

Processing of concurrent IRQ's

To service concurrence of IRQ's from several asynchronous signals, the PLC is equipped with the IRQ buffer register. If the requirement of the minimum interrupt period is not met, the stack may overflow and the IRQ may be lost. This state is signalled by the error message with the code 22 00 00 00 in registers S34 and S48 to S51. Gradual processing of IRQ's and prolongation of the response time of the program is illustrated in Fig. 10.5.

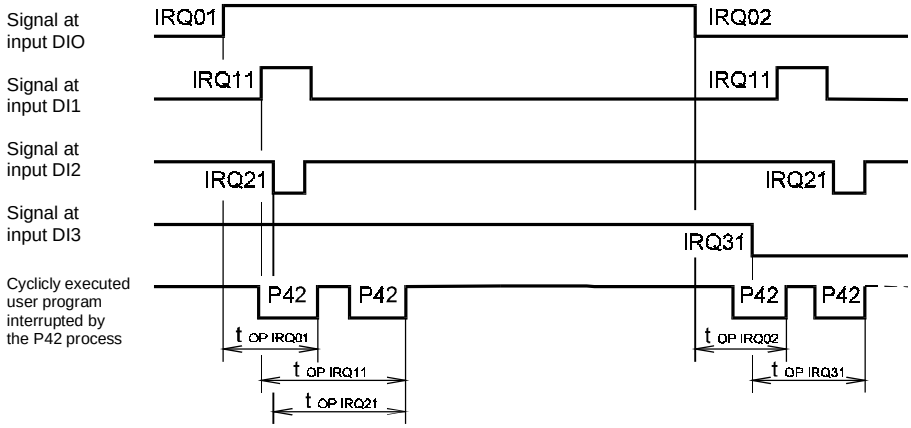


Fig. 10.5 Gradual processing of concurrent IRQ's

Prolongation of the user program cycle

When using interrupt inputs, it is necessary to keep in mind that evoking of interrupt processes causes prolongation of the program cycle time which may even lead to exceeding of the maximum allowed cycle time.

10.5.9 Servicing of the Type 3 Counter

Declaration of the type 3 counter

Declaration of the counter is performed by the directive `#unit` with the general structure according to item 10.5.2. Parameter `INITAB` of directive is mandatory. The initialization table serves for identification of the counter type. It contains one item only, constant 5.

Declaration example

```
#table byte IniCNT = 5    ;1 x unidirectional counter
;
#unit 0, 0, Count_600_, 3, 3, Xn, Yn, On, IniCNT
;
```

Parameter `TYP` of directive `#unit` is input symbolically `Count_600_` or numerically `$30`. Placement of the state and control word (parameters `Xn, Yn`) depends on the BM type (on occupation of the scratchpad by images of inputs and outputs).

Servicing of the type 3 counter

In the scratchpad memory, the counter occupies 3 bytes in image of inputs, and 3 bytes in image of outputs.

Image of inputs

The STAT state word is stored in the image of inputs and the current state of the counter. If the interrupt is allowed, image of inputs is updated before the P44 process is executed, if the interrupt is prohibited, it is updated in the cycle loop. Zone with the initial address defined by the parameter `Z_IN` of directive `#unit` has the following structure:

-	-	-	-	STAT .3	STAT .2	STAT .1	STAT .0	Z_IN
Less significant byte of the counter value								Z_IN+1
More significant byte of the counter value								Z_IN+2

The state word

STAT.0 = 1 - reaching of the maximum counter range (65535) in this cycle
STAT.1 = 1 - reaching of the pre-selection in this cycle
STAT.2 = 1 - reaching of the maximum counter range
The bit is set to zero by the zero level of the RESET signal or from the ascending edge of bit CONT.4
STAT.3 = 1 - reaching of the pre-selection
The bit is set to zero when the counter overflows, by zero level of the RESET signal or from the ascending edge of the CONT.4 bit
STAT.4 - state of the RESET input

Image of outputs

Image of outputs contains the CONT control word and the value of the counter pre-selection. State of bits CONT.5 to CONT.7 is accepted by the system after writing to the scratchpad, state of other bits in CONT as well as the pre-selection value, is accepted in the cycle loop, or at termination of the P44 interrupt process, respectively. Zone with the initial address defined by parameter `Z_OUT` of directive `#unit` has the following structure:

CONT .7	CONT .6	CONT .5	CONT .4	-	-	-	CONT .0	Z_OUT
Less significant byte of the counter pre-selection								Z_OUT+1
More significant byte of the counter pre-selection								Z_OUT+2

CONT.0 - blocking of the counter
0 = blocking of the counter
1 = counter running

CONT.4 - resetting of the counter
Change of the bit state from 0 to 1 performs reset of the counter and setting to zero of all bits of the STAT state word (while in state 1, the counter is not reset). Setting of the bit to zero is done by the user.

CONT.5 - control of the counter mode
0 = freely running counter
1 = self-filling counter with pre-selection

CONT.6 - allowing of interrupt from reaching of the maximum range
0 = interrupt prohibited
1 = interrupt allowed

CONT.7 - allowing of interrupt from reaching of the pre-selection
0 = interrupt prohibited
1 = interrupt allowed

Counter pre-selection

To determine the minimum value of the counter pre-selection in the self-filling mode and difference of values of two pre-selections following one after another of the freely running counter, the following relationship holds:

$$n \geq \frac{f\,[Hz]}{100}$$

n - value/difference of values of the pre-selection
f - frequency of signal at the CLK input.

Servicing within the P44 process

For servicing within the P44 process it holds that time of the interrupt process must not exceed 5 ms. It is also necessary to keep in mind that evoking of interrupt processes causes prolongation of the program cycle time which may even lead to exceeding of the maximum allowed cycle time.

Physical addressing of the counter

Reading of the state word, counter value, and writing of the control word and counter pre-selection can be performed by reading from and writing to the counter physical address.

```
LD     U$3000       ;reading of the STAT state word
LD     UW$3001      ;reading of the counter state

WR     U$3080       ;writing of the CONT control word
WR     UW$3081      ;writing of the counter pre-selection
```

The physical address has no automatic bond to the scratchpad

By reading from the physical address or writing to the physical address of the counter, the corresponding change of the value in image of inputs or outputs in the scratchpad memory does not happen!

In the case of physical reading, value in image of inputs is corrected in the course of the cycle loop.

In the case of physical writing, it is necessary to ensure the correction in the scratchpad by the user program otherwise in the cycle loop the counter will be set according to the original value in image of outputs.

Time diagrams of the counter modes

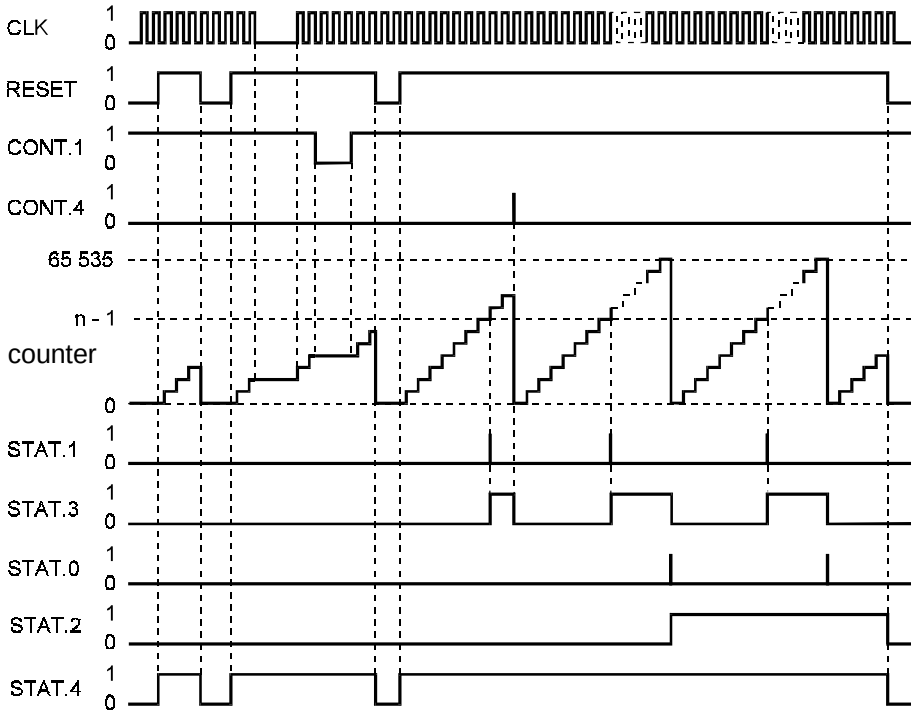


Fig. 10.6 Time diagram of the freely running counter

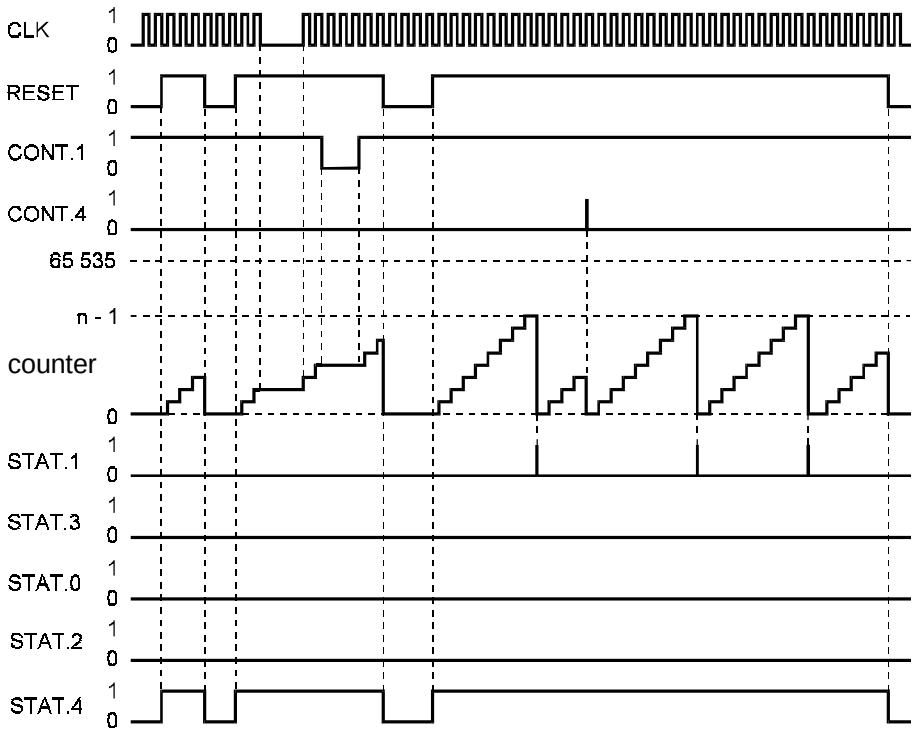


Fig.10.7 Time diagram of the self-filling counter with pre-selection

10.5.10 Incremental Encoder Servicing

Declaration of admeasuring

Declaration of admeasuring is performed by the directive `#unit` with general structure according to item 10.5.2.

Declaration example

```
#unit 0, 0, IRC_600, Xn, Yn, On
```

Parameter `TYP, POC_IN, POC_OUT` of directive `#unit` is input symbolically as `IRC_600` or numerically `$40, 5, 9`. Placement of the state and control word (parameters `Xn, Yn`) depends on the BM type (on occupation of the scratchpad by images of inputs and outputs).

Servicing of admeasurement Image of inputs

Admeasuring occupies the total of 14 bytes in the PLC scratchpad memory, 5 bytes in the image of inputs and 9 bytes in the image of outputs.

In the image inputs, the STAT state word is stored and the actual state of the admeasured value. If interrupt is allowed, image of inputs is updated before the start of the P44 process, or in the cycle loop if interrupt is prohibited. Zone with the initial address defined by the parameter `Z_IN` of directive `#unit` has the following structure:

STAT .7	STAT .6	STAT .5	STAT .4	STAT .3	STAT .2	STAT .1	STAT .0	
Least significant byte of the admeasured value								Z_IN
								Z_IN+1
								Z_IN+2
								Z_IN+3
Most significant byte of the admeasured value								Z_IN+4

The state word

STAT.0 = 1 - overflow of the maximum admeasurement range in this cycle (values 7FFF FFFFh)

STAT.1 = 1 - underflow of the minimum admeasurement range in this cycle (values 8000 0000h)

STAT.2 = 1 - reaching of pre-selection for the ascending direction in this cycle

STAT.3 = 1 - reaching of pre-selection for the descending direction in this cycle

STAT.4 - immediate movement direction
0 = ascending (from lower values to the higher ones)
1 = descending (from higher values to the lower ones)

STAT.5 - flag of the mode of the reference point look up
0 = passive mode
1 = active mode

STAT.6 - reaching of pre-selection for the ascending direction
0 = admeasured value below pre-selection
1 = admeasured value above pre-selection
The bit is set to zero at overflow of the maximum admeasurement range.

STAT.7 = - reaching of pre-selection for the descending direction
0 = admeasured value above pre-selection
1 = admeasured value below pre-selection
The bit is set to zero at underflow of the minimum admeasurement range.

The admeasured value

Admeasurement registers every edge of the phase-shifted incremental encoder signals, that means that the **admeasured value is the quadruple of the number of pulses of the generated incremental encoder's**. For example, in one incremental encoder loop with division into 1250 scale divisions, addition of the admeasured value is 5000.

Image of outputs

Image of outputs contains the CONT control word, pre-selection of the admeasured value for the ascending direction, and pre-selection of the admeasured value for the descending direction. State of bits CONT.6 and CONT.7 is accepted immediately after their writing to the scratchpad, state of other bits in CONT as well as of the pre-selections is accepted in the cycle loop, or upon termination of the P44 interrupt process, respectively.

CONT .7	CONT .6	-	-	-	-	CONT .1	CONT .0	Z_OUT
Least significant byte of pre-selection for the ascending direction								Z_OUT+1
Most significant byte of pre-selection for the ascending direction								Z_OUT+4
Least significant byte of pre-selection for the descending direction								Z_OUT+5
Most significant byte of pre-selection for the descending direction								Z_OUT+8

The control word

CONT.0 - mode of the reference point look up
Change of state of the bit from 0 to 1 evokes request for look up of the reference point (zero pulse). Setting of the bit to zero is done by the user. During look up of the reference point, the STAT.5 is set. The first zero pulse after accepting of the request, causes setting to zero of the admeasured value and the STAT.5 bit.

CONT.1 - admeasurement reset
Change of state of the bit from 0 to 1 evokes setting to zero of the admeasured value. During state 1, admeasurement is not reset.

CONT.6 - allowing of interrupt from overflow or underflow of the admeasurement range
0 = interrupt prohibited
1 = interrupt allowed

CONT.7 - allowing of interrupt from reaching of one of the pre-selections
0 = interrupt prohibited
1 = interrupt allowed

Pre-selection of the admeasured value

Pre-selections for both admeasurement directions may take arbitrary combinations of positive as well as negative values. For determining of the minimum difference of two pre-selection values following one after another, the following relationship holds:

$$n \geq \frac{f\ [Hz]}{400}$$

n - difference of two pre-selection values following one after another
f - frequency of the incremental encoder signal (given by division of incremental encoder and the movement speed)

Servicing in the P44 process

In servicing in the P44 process, it holds that the time of the interrupt process must not exceed 5 ms. It is also necessary to keep in mind that evoking of interrupt processes causes prolongation of the program cycle time, which may even lead to exceeding of the maximum allowed cycle time.

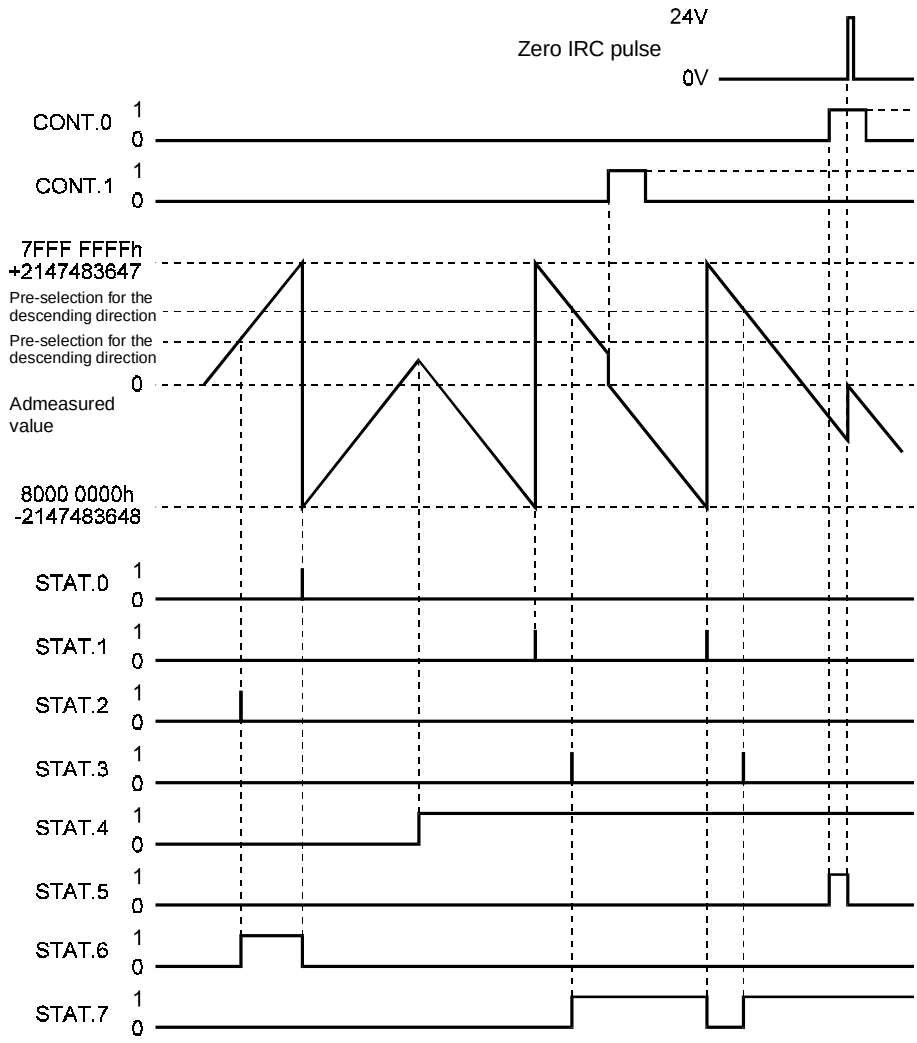


Fig.10.9 Time diagram of admeasuring using incremental encoder

10.5.11 Measurement of the Signal Period and Phase Shift

Function declaration

The function declaration is performed by the directive `#unit` with general structure according to item 10.5.2.

Declaration example

```
#unit 0, 0, Period_600, Xn, X_On ;measurement of the TC600
                                 ;period and phase shift
```

Parameter `TYP, POC_IN, POC_OUT` of directive `#unit` is input symbolically as `Period_600` or numerically `$50, 2, 0`.

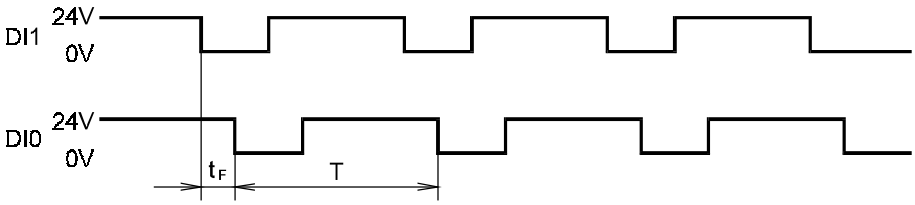
Placement of the function output (parameter `Xn`) depends on the programmable controller type (occupation of the scratchpad by images of inputs and outputs).

Servicing of the function

Both measurement modes occupy in the image of inputs of the PLC scratchpad memory 2 bytes at address defined by the parameter `Xn` of directive `#unit`. A content of the image is updated in the user program cycle loop.

In measurement of the signal period, these 2 bytes have the meaning of the number of cycles of the internal clock signal per 1 period of the measured signal. In measurement of the phase shift, they have the meaning of the number of cycles of the internal clock signal between two descending edges of the measured signals.

Graphic illustration of time of the period and phase shift



T signal period time at BM input DI0
t_F phase shift of signals at BM inputs DI1 and DI0

Measurement mode control

Control of the measurement mode is done by a program using the image of the binary output DO0 of BM (by image Yn.0).

If the bit Yn.0 = 0, measurement of the signal period is performed at input DI0 of BM, if the bit Yn.0 = 1, measurement of the phase shift of signals between inputs DI1 and DI0 of BM is performed.

Physical output DO0 of BM can be used only for indication of the function mode.

Period measurement

In signal period (frequency) measurement, it is possible to measure the signal within the frequency of about 1 Hz to 1 kHz. The measured number of cycles of the clock signal then reaches values of 32767 to 33. The value 65535 signals exceeding of the measurement range (it corresponds with the input signal frequency lower than 1 Hz, or possibly with a non-connected input).

For conversion of the number of cycles of the internal clock signal to the time information, the following relationship holds:

T [µs] = n x 30.5175

T signal period time at input DI0 of BM
n contents of two bytes of the scratchpad determined by the parameter `Xn` of directive `#unit`

In the case of measurement of a sine alternating signal period, doubling of frequency occurs at the input circuits (two-directional rectifying) and the measured period value corresponds with the half of its real value at input DI0 of BM.

Example of the period rectification

```
#program period
;
#unit 0, 0, Digit_600, 2, 2, X0, Y0, On     ;binary inputs
#unit 0, 0, Period_600, X2, X_On           ;period meter
;
#def Time XW2                    ;signal period in clock
cycles
#def cons1 30.5175         ;const. of conversion cycles -> µs
#def cons2 0.000001        ;const. of conversion µs -> s
;
#reg float Period,         ;signal period in µs
           Frequency              ;signal frequency in Hz
;
P 0
      LD     0
      WR     Y0.0          ;period measurement
;
      LD     Time
      UWF
      MUF    cons1
      WR     Period        ;period in µs
;
```

```
      LD    1
      UWF
      LD    Period
      MUF   cons2
      DIF
      WR    Frequency    ;frequency = 1 / period
E 0
```

Phase shift measurement

Measurement of the phase shift is used for signals with the same frequency. The time difference between descending edges of two different signals connected to inputs DI1 and DI0 of BM is measured. The measured number of cycles of the clock signal then reaches values of 1 to $\frac{T[\mu s]}{30.5175}$.

For conversion of the number of cycles of the internal clock signal to the time value, the following relationship holds:

$$t_F\,[\mu s] = n \times 30.5175$$

t_F phase shift of signals at inputs DI1 and DI0 of BM
n contents of two bytes of the scratchpad determined by the parameter `Xn` of directive `#unit`

In the case of measurement of phase shift of alternating signals, it is necessary to rectify the signals in single wave.

Example of the phase shift measurement

```
#program phase
;
#unit 0, 0, Digit_600, 2, 2, X0, Y0, On     ;binary inputs
#unit 0, 0, Period_600, X2, X_On           ;phase meter
;
#def Time XW2                    ;signal phase shift in clock
cycles
#def cons1 30.5175        ;const. of conversion cycles -> µs
;
#reg float Phase          ;signal phase shift in µs
;
P 0
      LD    1
      WR    Y0.0          ;phase shift measurement
;
      LD    Time
      UWF
      MUF   cons1
      WR    Phase         ;phase shift in µs
E 0
```

Physical addressing

Reading of the immediate value of the meter of frequency and phase shift can be done by reading with the physical address:

```
      LD    UW$5000       ;reading of the value of the meter
                          ;of frequency or phase shift
```

10.5.12 Physical Addresses of Inputs and Outputs

Structure of the physical address

Physical address of binary and analog inputs and outputs has the following structure:

address upper byte								address lower byte							
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

A15 to A12 - type of input and output (fixed-given)
1000 ($8) - binary inputs and outputs
1001 ($9) - binary inputs and outputs
1010 ($A) - binary inputs and outputs
1101 ($D) - analog inputs and outputs
other combinations are reserved

A11 to A8 - module type
0 - BM
1 - first EM/2
2 - second EM/2 or EM

A7 - address type
0 - input address
1 - output address

A6 to A0 - number of the input or output PLC byte

Use of the physical address in the U operand

The physical address is entered immediately after the U operand (or UW, respectively), always in the hexadecimal form.

```
LD     U$A000       ;direct reading of state of 8 bin. inputs
                    ;(byte 0)
LD     UW$A000      ;direct reading of state of 16 bin.
                    ;inputs (byte 0,1)
WR     UW$A080      ;direct writing of the value of 16 bin.
                    ;outputs (byte 0,1)
```

Physical address has no automatic bond to the scratchpad

By reading from the physical address or writing to the physical address of inputs and outputs, the corresponding change of value in image of inputs or outputs in the scratchpad memory does not happen!

In the case of physical reading, value in image of inputs is corrected in the course of the cycle loop, and usually this is faulty (however, it must to be taken into account).

In the case of physical writing, it is necessary to ensure correction in the scratchpad by the user program, otherwise in the cycle loop the outputs will be set according to the original value in the image of outputs.

Another possibility is to turn off servicing of PLC outputs in the software configuration in the compiler at compilation of the user program (item of the directive *#unit*) and service the outputs exclusively by direct writing using the U operand and the physical address.

10.6 Testing of Input and Output Signals

Procedure for testing of correct connection of input and output signals

For testing of input and output signals connected to the PLC, it suffices to create an empty program containing only sw configuration of the tested PLC and instructions P0 and E0 which create an empty basic process. Afterwards it is possible to observe states of the connected inputs using debugging means of the development environment and set arbitrary values at the PLC outputs. This very simple but very efficient procedure is recommended to be used before debugging of one's own user program as in this way the whole route from input elements (end switches, ...) through inputs and to the PLC scratchpad memory is verified in advance, as well as backwards, from the scratchpad memory through outputs and to the action elements. Errors arisen from connecting of the PLC to the controlled object can be removed in this way, finding of which is usually much more complicated in the phase of debugging of the control program.

10.7 Instruction Set

The set of instructions and system services of PLC's of the TC600 series is compatible with other Tecomat PLC's. The central unit of the D series contains the extended instruction set which, besides instructions of the reduced and standard instruction set, contains instructions designed form the most efficient PLC's.

Reduced instruction set

The following are parts of the reduced instruction set:

- bit logical operations
- basic operations of counters and timers
- basic organizational instructions and transfers in the program
- comparison in the extent of a word
- one-loop control

Standard instruction set

Compared to the reduced instruction set, the standard instruction set contains the following in addition:

- logical operations in the extent of a byte and word
- extended operations of counters, timers, shift registers
- arithmetic instructions, conversions and comparison in the extent of a word
- extended organizational instructions, transfers in programs
- table instructions above tables in the user memory which allow for optimum realization of even very complicated combination and sequence function blocks, decoders, time and sequence controllers, sequence generators, furthermore they make easier realization of diagnostic functions, recognition of error states, sequence records of events, protocols about the process, diagnostic messages of the type "black box"
- table instructions above the space of variables allow for operation with indexed variables, realization of the delay line, long shift registers, conversions to the code "1 of n", selection of variables, step controllers, records of events and various stack structures
- instructions of the sequence controller
- instructions realizing the set of logical operations, including counting of ones bits in the operand of the word type. In this way it is possible to easily realize the majority and general threshold functions, parity functions (MOD 2), and arbitrary symmetric functions
- 8 user stacks and instructions for their switching which allow for transfer of more parameters among functions which do not follow immediately one after the other, storing of the immediate state of the stack, etc.
- automatic conversion of the length of operands and intermediate results in combination of bit, byte and word instructions or logical instructions with arithmetic ones
- system variables in which the system time is realized, system time units and their edges, communication variables, flag and command variables, system messages
- multiprogramming (multi-loop control) including interrupt processes which contributes to shortening of the response time as well as to easier programming
- user instructions USI which realize in the optimum way (on the level of the microprocessor instructions) complex tasks (special communication, regulation, time-critical user tasks)

Extended instruction set

Compared to the standard instruction set, the extended instruction set contains the following in addition:

- logical operations in the long extent
- arithmetic instructions, conversions and comparisons in the long extent
- conditional jumps according to the comparison flags
- arithmetic instructions in the format with the floating point
- extended table instructions with tables of large extent
- table instructions with structuralized access
- instructions of the PID regulator

Full description of the instruction set is given in the handbook *Instruction Set of Tecomat PLC, TXV 001 05.02*

11. Diagnostics and Removal of Faults

The PLC diagnostic system

The Tecomat PLC diagnostic system is a part of the standard sw and hw equipment of the PLC's. It is active starting from turning on of the PLC power supply and operates independently of the user. The main function is ensuring of error-free and accurately defined function of the PLC in any situation. The system continuously follows vitally important parts and functions of the PLC and ensures servicing of an error state immediately in the moment of its occurrence and informs about the fault.

In the case a fault arises within the PLC, the diagnostic system must especially eliminate the possibility of origination of breakdown states in the technology connected to the PLC.

Another task of the diagnostic system is to make easier removal of the arise fault to service workers or to the user, respectively.

Besides basic functions, the diagnostic system notifies the user of any possible erroneous manipulations or procedures at the PLC attendance due to which working with the PLC becomes easier and more efficient.

11.1 Conditions for Proper Function of the Diagnostics

The basic condition for error-free function of the PLC and proper operation of its diagnostics is proper functions of the power supply and of the central unit.

After turning on of the supply, basic checking of the system kernel is performed within the initialization. If an error of the EPROM or RAM system memory is found, the diagnostic system cannot continue in its operation. This state is signalled by lighting the letter E or t on the display.

11.2 Indication of Errors

Error stacks

The central unit is equipped with the main error stack which contains 8 last error codes announced by the diagnostics of the whole PLC and a local stack containing 8 last error codes announced by the diagnostics of servicing of inputs, outputs, and communication through the serial channels.

Indication of errors

Full error code in the main error stack is 4 bytes long. The first byte gives the basic error code (it determines the group of faults), the following 3 bytes give close specification of the error.

Full error code in the local error stack is 2 bytes long. The first byte gives the basic error code (it determines the group of faults), the second byte gives closer specification of the error.

Contents of both error stacks are available from the xPRO development environment. Codes of serious errors are shown on the display at the moment of their evaluation in the format:

E - 80 - 09 - 00 - 00

E - label followed with the full error code in hexadecimal form
80 - basic error code
09 00 00 - closer error specification

11.3 Serious Errors

PLC behaviour in the case of a serious error

In the case of the rise of a serious error, the diagnostic system blocks the outputs first, interrupts execution of the user program, and then it identifies the arisen fault. The full error code is shown on the display and stored in the main error stack.

Indication of such an error can be cancelled by a command from the superior system or by turning off and on of the PLC power supply.

The following abbreviations and terms are used in the overview of error codes:

PC - address of instruction in which the error occurred (program counter)

AM - activation of inputs and outputs:
$40 = activation of inputs
$80 = activation of outputs
$C0 = activation of inputs and outputs

AJ - upper byte of the physical address of inputs and outputs at which the error occurred
$12 = serial channel CH2
$13 = serial channel CH3
$81 = binary inputs and outputs of the first EM/2 (TC631, TC632)
$82 = binary inputs and outputs of the second EM/2 (TC631, TC632)
$91 = binary inputs and outputs of the first EM/2 (TC633)
$92 = binary inputs and outputs of the second EM/2 (TC633)
$A0 = BM binary inputs and outputs
$A2 = EM binary inputs and outputs
$D0 = BM analog inputs and outputs
$D1 = analog inputs of the first EM/2
$D2 = analog inputs of the second EM/2 or EM

Map of the user program
- main control structure generated by the compiler.

Numerical codes are given in the hexadecimal form.

11.3.1 User Program Errors

Errors of storage of the user program

80 01 00 00	wrong length of the user program map in the EEPROM source memory
80 02 00 00	wrong ensuring character (CRC) of the user program map in the EEPROM source memory
80 03 00 00	wrong ensuring character (CRC) of the whole program in the EEPROM source memory
80 04 00 00	user program is not in the EEPROM source memory Fault in the EEPROM source memory has occurred, the user program is designed for another series of central units or it has not been recorded in the EEPROM at all. It is necessary to load a new user program in EEPROM or disconnect the EEPROM memory and load the user program in the RAM memory.
80 05 00 00	wrong length of the user program map in RAM
80 06 00 00	wrong ensuring character (CRC) of the user program map in RAM
80 07 00 00	wrong ensuring character (CRC) of the whole program in RAM A fault in the memory has occurred. It is necessary to load a new user program in RAM.
80 08 00 00	editing intervention in the user program while the EEPROM source memory has been connected If the EEPROM memory is connected, after turning on the system its contents is loaded in the RAM memory of the central unit. The central unit checks integrity of the program copy from EEPROM. In the case of editing intervention, it announces the error Editing intervention, and it is necessary to disconnect the EEPROM memory or re-program it. If the editing intervention has been unwanted, it is sufficient to turn off the PLC and turn it on again, and the original program will be loaded from EEPROM.

	80 09 00 00	the program has been compiled for another series of central units The compiler was set for another series of central units. It is necessary to select the correct series of central units in the compiler menu (the series is marked by a capital letter in the name of the central unit) and compile the user program again. If the compiler was set correctly, then this compiler is designed for higher version of the system sw than the version fitted in the central unit of your PLC. This dissonance must be removed either by using an older version of the compiler or by exchanging of the system sw in the CPM.
	80 0A 00 00	attempt to program a non-existent EEPROM The memory is not fitted or is disconnected.
	80 0B 00 00	programming of EEPROM was unsuccessful
	80 0C 00 00	failure of the RTC real time circuit The real time circuit is not functions the consequence of which is failure of all time functions of the PLC. The most likely fault is discharge of the backing battery which must be exchanged. If the backing battery is not discharged, an expert repair of the central unit is necessary.
	80 0F 00 00	memory of CPU parameters cannot be programmed
	80 0F 01 00	memory of CPU parameters cannot be retrieved
Programming errors	80 10 PC PC	overflow of the stack of return addresses The maximum number of nested subprograms has been exceeded. Nesting means calling of another subprogram from within the subprogram being already executed.
	80 11 PC PC	underflow of the stack of return addresses Return instruction from a subprogram (RET, RED, REC) was not preceded by calling of the subprogram (CAL, CAD, CAC, CAI).
	80 12 PC PC	non-zero stack of return addresses after the process termination In the user program, there is a different number of instructions of calling of the subprogram (CAL, CAD, CAC, CAI) than return instructions from the subprogram (RET, RED, REC).
	80 13 PC PC	label not declared The instruction of jump or calling with a label number has been used which is not used anywhere in the user program.
	80 14 PC PC	the label number is greater than the maximum value Number of label of an instruction of jump or calling is greater than the greatest number of label used in the user program.
	80 15 PC PC	table T not declared Table T used in this instruction has not been input in the user program. It must be added.
	80 16 PC PC	unknown instruction code The used instruction is not implemented in this central unit.
	80 17 PC PC	irregular user instruction USI The user instruction is intended for another series of central units or its structure is broken.
	80 18 PC PC	the requested user instruction USI does not exist The requested user instruction USI is not connected to the user program.

80 19 PC PC error of BP instructions nesting

The BP instruction cannot be used in processes P50 to P57 (calling of the debugging process P5n in another P5m process).

80 1A PC PC process for servicing of the BP is not programmed

The debugging process P5n called by the BP instruction is not programmed. It is necessary to add it to the user program.

80 1B PC PC wrong configuration of table T

The checksum of values of table T used by this instruction does not agree. The user program must be loaded again.

80 30 00 00 exceeding of the maximum cycle time

The cycle time has been longer than the input value.

80 31 00 00 exceeding of the maximum interrupt process time

Execution time of the interrupt process has exceeded 5 ms or the cycle time has been exceeded in the course of the interrupt process execution (see error 80 30 00 00).

11.3.2 Errors in the Peripheral System

Errors of sw configuration

81 00 30 AJ

30 AJ exceeding of the number of bytes in the PLC

Greater number of bytes has been input in the user program sw configuration than the PLC actually occupies. This entry must be corrected and the corrected program must be loaded in the PLC again.

81 00 31 AJ

31 AJ initialization table is missing

Initialization table is missing in the user program, which is necessary for servicing of some types of the PLC inputs and outputs (for example, analog inputs, special functions, etc.). This table must be added to the user program and the corrected program must be loaded in the PLC again.

81 00 32 AJ

32 AJ unknown servicing

The central unit cannot service this type of the PLC inputs or outputs. The system program must be exchanged for a newer version (the version number can be found out either in the xPRO program or from the PLC display after turning on of the power supply).

81 00 33 AJ

33 AJ odd number of bytes for analog inputs

In the user program sw configuration, an odd number of bytes has been input for analog inputs which is not allowed because one input takes two bytes. This entry must be corrected and the corrected program must be loaded in the PLC again.

81 00 34 AJ

34 AJ wrong number of bytes of the initialization table

The initialization table has a different number of bytes than its servicing requires. The table must be corrected and the corrected user program must be loaded in the PLC again.

81 00 35 AJ

35 AJ overfilling of the initialization zone

		A part of memory in the central unit reserved for initialization data of the given type of inputs or outputs has been overfilled.
	81 00 36 AJ	
	36 AJ	number of the initialization table is greater than the maximum allowed value
		Number of the initialization table is greater than the central unit allows. The table number must be corrected and the corrected program must be loaded in the PLC again.
	81 00 37 AJ	
	37 AJ	wrong configuration of the initialization table
		The checksum of values of the initialization table does not agree for this type of inputs or outputs. The user program must be loaded again.
	81 EM 38 AJ	
	38 AJ	wrong entry in the initialization table
		There is a wrong entry in the initialization table. At initialization of serial channels, this is usually due to exceeding of the maximum allowed value of a parameter (for example, length of the transmitted data).
Errors of inputs and outputs during operation	81 00 40 AJ	
	40 AJ	inputs did not report themselves
		PLC inputs stopped to report themselves. The likely cause is a fault at the address decoder of the input and output unit or the connection with the CPU is faulty.
	81 00 41 AJ	
	41 AJ	outputs did not report themselves
		PLC outputs stopped to report themselves. The likely cause is a fault at the address decoder of the input and output unit or the connection with the CPU is faulty.
	81 00 43 AJ	
	43 AJ	use of non-existent inputs or outputs
		Servicing of non-existent inputs or outputs has been run. The most likely cause lies in co-operation of the superior PC's programming software and the PLC central unit.
Errors of hw configuration	81 00 61 00	
	61 00	overflow of the zone for inputs configuration
	81 00 61 01	
	61 01	overflow of the zone for outputs configuration
		These errors are caused by too large number of types of inputs or outputs written in the sw configuration in the user program. The maximum numbers are 16 types of inputs and 16 types of outputs including special functions.
	82 06 AM AJ	error of configuration
		A declared type of inputs or outputs has not been found.

11.4 Other Errors

In the case of origination of some of other errors which do not essentially affect the control itself, the diagnostic system only identifies the arisen fault, announces the basic error code in the S34 register, and the full error code in registers S48 to S51, and control of the process runs further. The information can be used for user treatment of these errors.

The error can also be found by reading of the error stack into the superior system (PC).

11.4.1 Errors of Serial Communication

This group of errors is written only to the local stack without the possibility of evaluation by the user program.

Errors of the serial communication protocol

10 05	wrong start delimiter
11 05	SD parity error
11 06	LE parity error at SD2
11 07	LER parity error at SD2
11 09	DA parity error at SD2
11 0A	SA parity error at SD2
11 0B	FC parity error at SD2
11 0C	RB parity error at SD2
11 0D	DAT parity error at SD2
11 0E	CHS parity error at SD2
11 0F	ED parity error at SD2
11 10	DA parity error at SD1
11 11	SA parity error at SD1
11 12	FC parity error at SD1
11 13	CHS parity error at SD1
11 14	ED parity error at SD1
12 07	different value of LE and LER - SD2
13 08	different value of SD and SDR - SD2
14 0A	extended address SA - cannot be processed- SD2
14 11	extended address SA - cannot be processed- SD1
15 0B	error of receiving flag FCF in control byte FC - SD2
15 12	error of receiving flag FCF in control byte FC - SD1
18 0E	wrong checksum CHS - SD2
18 13	wrong checksum CHS - SD1
19 0F	wrong end delimiter ED - SD2
19 14	wrong end delimiter ED - SD1

These errors are caused by excessive disturbances of the serial communication. They cause loss of the message and the consequence of their more frequent occurrence is even disconnection of the communication.

Error 10 05 or some of errors of group 11 may arise on the one-time basis at establishment of communication with the superior system in the middle of a message being transmitted by this system. If such errors no more occur in the course of further communication, everything is correct.

Errors from the CH2 serial channel have the value of the second byte increased by 20 (for example, error 10 25, etc.).

20 FC	wrong control byte in combination with a global address
2X RB	unknown communication function (X is the value of the control byte FC - 3, 4, 5, 6, 9, C, D, E, F)

The PLC does not know the requested communication function. The system program must be exchanged for a newer version (version number can be found either in the xPRO program or on the PLC display after turning on of the power supply).

11.4.2 System Errors

Using registers S34 and S48 to S51, these errors can be treated as needed by the user program.

System errors

07 00 00 00 error at checking of the remanent zone

The backed part of the scratchpad, the so called remanent zone, has wrong checksum. Cold restart will be performed. The cause is a fault in backing of the RAM user memory on the central unit, the most likely fault is at the backing battery.

08 00 00 00 exceeding of the first limit of guarding the cycle time
The cycle time has been longer than the set warning value.

09 00 00 00 wrong system time of the RTC circuit
The current time must be written from the superior system.

11.4.3 User Program Errors

These errors can be treated as needed in the user program either by eliminating the cause by checking input parameters before executing of the given instruction or by treating the consequence.

Programming errors

10 00 00 00 division by zero
Divisor in the division instruction equal to 0.

11 00 00 00 initial index for WMS instruction lies outside of table T
WMS instruction has a wrong parameter and therefore it will not be executed.

12 00 00 00 initial index for LMS instruction lies outside of table T
LMS instruction has a wrong parameter and therefore it will not be executed.

13 00 00 00 table instruction above the scratchpad has exceeded its range
Table defined by the table instruction above the scratchpad has exceeded its range. Instruction will not be executed.

14 00 00 00 source block of data defined outside of the range
Source block of data for the move instruction has been defined outside the range of the scratchpad, data or table. Instruction will not be executed.

15 00 00 00 target block of data defined outside of the range
Target block of data for the move instruction has been defined outside the range of the scratchpad or table. Instruction will not be executed.

11.4.4 Errors in the Peripheral System

22 00 00 00 overflow of the internal stack from interrupt inputs

40 00 50 00 overloaded outputs

11.5 Solution of Communication Problems with the Superior System

Connection of the PLC to a superior system, usually a PC, is a necessity as every PLC must be programmed. Possible problems and way of their analysis is indicated on the following lines.

Checking of the PLC

1. **Is the power supply led to the PLC?**
   No Correct the situation.
   Yes ↓
2. **Has the PLC passed the starting sequence and is in the RUN mode or HALT?**
   (see Article 10.3)
   No An error has occurred in testing of the system kernel, communication is not possible, it is necessary to repair the PLC.
   Yes ↓
3. Do you want to program the PLC using the xPRO development environment?
   No Continue at item 5.
   Yes ↓
4. **Do you use channel CH1 for programming?**

No **CH1 must be used for the PLC programming, correct the situation.**

Yes Continue at item 6.

5. Do you use channel CH1 for connection?

No Continue at item 10.

Yes ↓

6. Do you use the standard-fitted CH1 RS-232 interface for communication?

No Continue at item 9.

Yes ↓

7. Do you use CH1 output at connector L?

No CH1 RS-232 interface is led out to connector L, correct the situation.

Yes ↓.

8. Do you use the interconnection cable TXK 646 51.06?

No Check connection of your cable.

Yes Continue at item.

9. Do you use CH1 output at terminal board K?

No CH1 optional interface is led out to terminal board K, correct the situation.

Yes Continue at item 11.

10. Do you use CH2 output at terminal board N?

No CH2 interface is led out to terminal board N, correct the situation.

Yes ↓.

11. Are parameters of the relevant channel set properly?

No Set the parameters (see Article 4.5)

Yes In the case of using CH1 RS-232 or CH2, continue at item 14.
In the case of using the CH1 optional interface ↓

Checking of the serial interface converter

12. Is the interface converter applied?

No Continue at item 14

Yes ↓

13. Is the interface converter equipped with indication of the power supply and state of signals?

No Consider all following possibilities.

Yes, no signal diode is lighted.
Power supply of the converter is not on or the converter is damaged.

Yes, only POWER is lighted.
Error in the PLC or in the cable between the PC and the converter.
Continue at item 14.

Yes, during the data transmission, only TxD blinks, RTS is lighted either permanently or is not lighted at all.
Fault of the RTS signal between the PC and the converter or the PC does not support control of the RTS signal necessary for the RS-485 interface (for RS-232 and RS-422 it is not necessary).
If the software of the PC does not support the RTS signal, it is necessary to set the converter in the mode of automatic switching of the communication direction, and to set sufficient reply delay at the central unit (see Article 4.5).
Development environments xPRO, EPOS and some visualization programs support the RTS signal.

Yes, during the data transmission only TxD and RTS blink.
Fault at the output part of the converter, in the cable between the controller and the PLC, or possibly in the PLC.

Yes, during the data transmission TxD with RTS and RxD blink alternately.
Communication is correct, the fault is in the cable between the controller and the PC or in the PC.
Continue at item 14.

Checking of the cable

14. Is the cable inserted in the correct COM socket at the PC?

No Correct the situation.

Yes ↓

15. Are proper cables used?

No Correct the situation, check connection of cables of your own production.

Yes ↓

Checking of the PC

16. On which COM channel is the mouse installed and on which channel do you communicate?

The same one

Collision of drivers occurs even in the case that the mouse is not connected. It is necessary to communicate on another COM or to uninstall the mouse driver.

Mouse on COM1, communication on COM3

Mouse on COM2, communication on COM4

Mouse on COM3, communication on COM1

Mouse on COM4, communication on COM2

Some programs (for example, xPRO) cannot communicate on a channel which shares the same interrupt vector as the mouse driver. It is thus necessary to apply a different combination than one of those given above. In the xPRO program, in the communication options it is possible to set another interrupt vector. However, experiments of this type are intended for experienced PC users.

Other combinations ↓

Problem of falling-out communication

17. The whole line is in proper state but the PC does not receive the reply or the communication falls out often

The problem occurs in programs operating in protected mode or under operation system with graphical interface (Windows).

In the xPRO program which operates in the protected mode from version 2.1, PC serial channel equipped with an equivalent of circuit 16550 with buffer stacks is a necessity. Among communication options in the xPRO program, we then check the option UART 16550A and select *Interrupt - standard*. With the accession of the Windows 95 operating system, all new computers are standard-equipped with these circuits. Older computers can be either equipped with an additional board with serial channels (xPRO then communicates even on a PC with the 386SX processor) or select *Interrupt - standard* or *Interrupt - no interrupt* and gradually reduce the communication speed (the speed must be obviously reduced at the PLC central unit as well). The selection UART 16550A must not be checked. Reduction of the communication speed makes sense in PC's equipped with the processor 486DX or 486DX2 and better.

Some programs in the Windows environment cannot switch with sufficient speed from transmission to receiving. This problem can be easily solved by setting sufficient reply delay at the PLC central unit (see Article 4.5).

12. Removal of Faults

Within the guarantee period, repairs may be performed only by the producer's employee or by a service organization determined on the basis of an agreement.

PLC's of the TC600 series are complex electronic devices fitted with parts for printed mounting and parts sensitive to the electrostatic charge. Therefore the producer recommends to perform post-guarantee repairs only by exchanging the whole units. For localization of the fault, the PLC's are standard-fitted with the diagnostic system. Repairs of the units are performed by the producer.

13. Maintenance

When general conditions for the installation are met, the PLC requires minimum maintenance. Operations in which demounting of a part of the PLC is necessary, are performed always with the PLC power supply, inputs and outputs turned off.

13.1 Demounting of the PLC Parts

Removal of the BM and EM cover

The BM cover is formed by the cover of the inputs and outputs board and by the LED display cover. Cover of the inputs and outputs board can be removed after unscrewing 4 fastening screw, the LED display cover can be removed after unscrewing of 2 fastening screws.

EM and EM/2 covers (inputs and outputs boards) can be removed after unscrewing of 4 fastening screws.

Taking out of the inputs and outputs board

The inputs and outputs board can be taken out after unscrewing of 4 fastening screws. In the BM, the board is interconnected with freely demountable insertion connection with the CPU board.

Making accessible of BM optional piggybacks

Optional piggybacks are placed on the BM CPU board. To make them accessible, it is necessary to take out the mounting unit formed by the CPU board, the shielding cover and the inputs and outputs board. After removal of the BM covers and after unscrewing of 6 screws on the bottom side of the BM trough, the unit can be taken out by its shifting to the right (the shielding cover is inserted in 2 slots on the left side of the BM trough).

Parts sensitive to the electrostatic charge are used at the PLC units. Follow principles for working with these circuits in manipulation with the units.

13.2 Checking of PE Connectors Interconnection

Resistance between an arbitrary metal part of the PLC and the main protective connector of the case in which the PLC is placed, is measured by the meter of small resistances. Value of the resistance must be $\leq 0{,}1\ \Omega$

13.3 Checking of the Power Supply

The PLC power supply is measured at connectors marked as M1 and M2. The allowed voltage tolerance is 24 V~ ±20 %, 24 V- ±20 %.

13.4 Checking of Voltage of Binary Inputs

Voltage of binary inputs is measured between the common connector of the group (COM) and connectors of individual inputs (DI).

The allowed voltage tolerance for closing of the input is 15 V~ to 30 V~ or 16 V- to 30 V-. Allowed voltage tolerance for opening of the circuit is 0 V~ to 11 V~ or 0 V- to 12 V-.

Allowed voltage tolerance for closing of fast inputs (DI0 to DI3 of modules TC603 to TC607) is 17,5 V~ to 30 V~ or 18,5 V- to 30 V-. Allowed voltage tolerance for opening of the input is 0 V~ to 13,5 V~ or 0 V- to 14 V-.

13.5 Checking of Voltage of Binary Transistor Outputs

Voltage of binary transistor outputs is measured between connectors UDO and GND of the relevant group of outputs. Allowed voltage range is 9.6 V- to 28.8 V-.

13.6 Battery Exchange

Exchanging of the battery (Panasonic CR2032 or a similar lithium battery of 3 V, 210 mAh, ϕ 20 mm) can be performed without losing of the user program and set parameters in the following way:

- turn off the PLC and inputs and outputs power supply
- remove the BM cover
- disconnect jumper V1 (next to the battery)
- take out the battery (on the upper edge of the CPU board)
- insert a new battery
- connect jumper V1
- screw on the BM cover

When the battery is disconnected (jumper V1 is disconnected), memory of the user program and the RTC circuit are supplied for the period of about 5 minutes from the backing condenser.

Metal instruments which could short-circuit the battery (for example the tweezers, flat pincers etc.) must not be used to insert the new battery. Pay attention to correct polarity.

The recommended interval of the battery exchange is 5 years. For the way of indication of lower battery voltage see Article 4.2.

13.7 Fuse Exchange

The internal fuse of the voltage converter can be exchanged without demounting of the BM cover through a cut-out on the bottom side of the cover. Non-breaking of the fuse is signalled by the lighted green LED diode placed behind the fuse when the regulator power supply is on. Type and value of the fuse are given on the label close to the fuse. Exchange of the fuse is done with the PLC power supply turned off.

13.8 Cleaning

To clean the PLC, no solvents, diluents, alcohols or similar substances may be used. To clean the surface covered by labels, it is possible to use fabric imbued with some diluted detergent cleaning means. Cleaning of dusty units is performed by a stream of air.

14. The Guarantee

Guarantee and reclamation conditions follow the *Commercial Conditions of Teco a.s..*

Technical Equipment
of TC600
Programmable Logic Controller

Supplement

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1.1 Setting of CH1, CH2, CH3 serial communication channels parameters

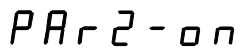
(extension of paragraph 4.5.1. of the basic manual)

Another parameter of CH1, CH2 and CH3 communication channels is introduced for TC600 PLC starting with the 7.4 version system program equipment. It is **parity mode** parameter. This parameter is set as the last parameter of the given channel.

The support of the piggyback MR-14, MR-15 of 1.6 version and higher is necessary for the CH3 channel moreover.

Setting of the parity mode

When setting the **parity mode** parameter the display shows the report of this type:



which has the following meaning:

PAR - setting of parity mode
2 - number of set cannel
on - parity switched on

Parity can be either switched on or off. In case of switched on parity it is always even parity. By pressing of „SET„ key, setting is changed, by pressing of „MODE„ the set value is stored and we pass to the following or previous parameter setting.

Parity is standardly switched on. It is switched off only the cases of necessity when it is necessary to communicate over modems, e.g., that do not transmit parity. By switching parity off security of transmitted data is decreased (for details see Serial communication of TECOMAT programmable logic controllers and TECOREG regulators, version 7 and higher, order number TXV 001 06.02 handbook).

Parity mode is set only for **PC** and **MAS** modes.